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     FILE 'WPIX, JAPIO' ENTERED AT 16:11:03 ON 24 APR 2002
L1      1085960 S BAR OR BARRICADE OR BARRIER OR BLOCKAGE OR CLOG OR CLOGG? HAM
L2      1968158 S CIRCUIT
L3      2539412 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT)) OR (MICRO)(W
L4       651342 S INITIALIZ? OR RESET? OR RESTART? OR FORMAT? OR REVAMP? OR REB
L5       461307 S CPU OR PROCESSOR OR (CENTRAL(2N)PROCESS?(2N)UNIT) OR CPUS
L6       597969 S PRINTER? OR(BUBBLE OR LASER OR INK)(2N)(JET OR JETS) OR LED O
L7        10652 S T01-C05A/MC
L8        17622 S L1(2N)L2
L9        17622 S L8 AND L3
L10        1900 S L9 AND L4
L11        1133 S L8 AND L5
L12        1133 S L9 AND L5
L13          83 S L12 AND (L7 OR L6)
L14          18 S L13 AND L4
L15        1900 S L8 AND L4
L16         221 S L15 AND L5
L17          18 S L16 AND L6
L18           0 S L16 AND L7
L19           0 S L17 NOT L14
L20      123800 S L3 AND L5
L21        1133 S L20 AND L8
L22         221 S L21 AND L4
L23         177 S L22 AND SIGNAL
L24          15 S L23 AND (L6 OR L7)
L25           0 S L24 NOT L14
L26       18138 S L5(2N)OUTPUT
L27          18 S L26 AND L23
L28          16 S L27 NOT L14
L29        1683 S (L6 OR L7) AND L26
L30         198 S L29 AND L4
L31          90 S L30 AND SIGNAL
L32           2 S L31 AND L8
L33           0 S L32 NOT (L17 OR L28)
L34          39 S L31 AND INPUT
L35          39 S L34 NOT (L17 OR L28)
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L14 ANSWER 1 OF 18 WPIX (C) 2002 THOMSON DERWENT
AN 1999-251629 [21] WPIX
DNN N1999-188239
TI Drive control apparatus of stepping motor for **printer** - has generator **circuit** which generates interruption signal to motor, when phase excitation value differs predetermined value.
DC T04 V06
PA (TODK) TOKYO ELECTRIC CO LTD
CYC 1
PI JP 11075398 A 19990316 (199921)* 8p
ADT JP 11075398 A JP 1997-234531 19970829
PRAI JP 1997-234531 19970829
AB JP 11075398 A UPAB: 19990603
NOVELTY - When the phase excitation value of the coil is different from a predetermined value, an interruption signal is output from a generator **circuit** (50) to **stop** the motor rotation. DETAILED DESCRIPTION - A controller (30) outputs control and designation signals as a pulse signal (SGN) to a stepping motor (10) through a driver (20). The pulse signal is input into each coil of stepping motor.
USE - For performing drive control of stepping motor in **printer**.
ADVANTAGE - Since an interruption signal is input when the drive source voltage falls below a predetermined value, the motor performs reliable operation even when unexpected service interruption is produced. Since the interruption signal is output based on the stop signal input from the **printer**, subsequent paper cutting operation is performed with stability. **Initialization** of the **CPU** is performed more reliably. DESCRIPTION OF DRAWING(S) - The figure shows **circuit** diagram of the control apparatus. (10) Stepping motor; (20) Driver; (30) Controller; (50) Generator **circuit**.
Dwg.1/6

L14 ANSWER 2 OF 18 WPIX (C) 2002 THOMSON DERWENT
AN 1999-088739 [08] WPIX
DNN N1999-065120
TI Low voltage protection method for e.g. laser **printer** - involves performing low voltage protection of operating voltage by **reset** signal output to **CPU** and overcurrent protective **circuit** of switch power supply.
DC P75 T01 T04 U13 U14 U21 U24
PA (CANO) CANON KK
CYC 1
PI JP 10323038 A 19981204 (199908)* 13p
ADT JP 10323038 A JP 1997-137413 19970513
PRAI JP 1997-137413 19970513
AB JP 10323038 A UPAB: 19990302
The method involves outputting a **reset** signal (129) for detecting operating voltage supplied to a **CPU** (127). The **CPU** is started from an initial stage depending on the detected voltage.
The **reset** signal and an overcurrent protective **circuit** (114) of a switch power supply, perform a low voltage protection of the operating voltage. Preferably, a **reset IC** (128) outputs the **reset** signal for starting the **CPU**.
ADVANTAGE - Reduces cost of low voltage protective **circuit** and ensures voltage detection accuracy by using existing over voltage or over current protective **circuits**. Enables **stopping** of

power supply during operation of **CPU**. Ensures effective and controllable low voltage protective device.
Dwg.1/12

L14 ANSWER 3 OF 18 WPIX (C) 2002 THOMSON DERWENT
AN 1998-529341 [45] WPIX
DNN N1998-412982
TI Logic analyser preprocessor **circuit** for 12C data - has two latch **circuits** for detecting start and stop conditions, with shift register to convert data into 9 bit parallel stream, together with associated counter.
DC T01 U21
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI RD 411087 A 19980710 (199845)* 1p
ADT RD 411087 A RD 1998-411087 19980620
PRAI RD 1998-411087 19980620
AB RD 411087 A UPAB: 19981111
The preprocessor device has START and STOP detection circuitry which comprises two stage latches, to detect the asynchronous START and STOP conditions. For the START condition, the first latch is set when the SCL and SDA bus conditions are high. The second latch is set when a low to high transition occurs on the SDA bus.

A 9 bit shift register converts the 8 bits of the 12C data, plus the acknowledge bit serial data stream, into a 9 bit parallel data stream that is fed to the analyser. A 9 bit counter is used to keep track of when the parallel data fed to the **processor** is valid. The counter is asynchronously **reset** when a START or STOP condition is detected, to **restart** the acquisition of the data. Two bicolour **LEDs** give a rapid indication of any activity occurring on the 12C bus, indicating the SCL and SDA states on the 12C bus, and providing feedback as to whether the 12C hardware allows the SCL and SDA signals to float high when a 12C transfer is complete.

USE - For debugging 12C interfaces.

ADVANTAGE - Creates logic analyser specifically for 12C bus, which is unavailable elsewhere.
Dwg.0/0

L14 ANSWER 4 OF 18 WPIX (C) 2002 THOMSON DERWENT
AN 1991-298167 [41] WPIX
DNN N1991-228460
TI Paging receiver reporting time of paging - has several **LED** selectively glowing or flashing in particular colour to indicate time of paging.
DC S04 W05
IN MOTOHASHI, T; SONE, T
PA (NIDE) NEC CORP
CYC 3
PI GB 2242770 A 19911009 (199141)*
AU 9173983 A 19911003 (199150)
AU 639991 B 19930812 (199339)
GB 2242770 B 19940105 (199401) 2p
US 5546078 A 19960813 (199638) 18p
ADT GB 2242770 A GB 1991-6687 19910328; AU 639991 B AU 1991-73983 19910328; GB 2242770 B GB 1991-6687 19910328; US 5546078 A Cont of US 1991-675511 19910327, Cont of US 1992-964462 19921015, US 1994-333744 19941103
FDT AU 639991 B Previous Publ. AU 9173983
PRAI JP 1990-33063U 19900329
AB GB 2242770 A UPAB: 19930928

The paging receiver comprises a timepiece for indicating the time of paging when the paging signal is received; reporting **circuit** for reporting the time of paging; and control **circuit** responsive to the time of paging for causing the reporting **circuit** to report the time of paging. The reporting **circuit** comprises a set of light emitting diodes (**LEDs**), the control controlling the **LEDs** such that, among the **LEDs**, a predetermined combination of **LEDs** matching the time of paging is selected and caused to glow in a predetermined colour.

The paging receiver further comprises **stopping circuit** for causing the reporting **circuit** to **stop** reporting the time of paging, and a time setting **circuit** for setting the timepiece **circuit** at a given time, and timepiece starter for causing the timepiece **circuit** to start counting time.

ADVANTAGE - Does not limit sensitivity with **CPU**, preventing need for LCD display.

3/19

L14 ANSWER 5 OF 18 WPIX (C) 2002 THOMSON DERWENT
AN 1989-326197 [45] WPIX
DNN N1989-248311
TI Page **printer** with temporary stop direct memory access - has interrupt controller that selects certain requests enabling fast servicing by **CPU**.
DC T01 T04
IN SUZUKI, M O
PA (HUGA) HUGHES AIRCRAFT CO; (OKID) OKI ELECTRIC IND CO LTD
CYC 4
PI EP 340972 A 19891108 (198945)* EN 17p
R: DE FR GB
US 4953103 A 19900828 (199037)
EP 340972 A3 19920513 (199330)
ADT EP 340972 A EP 1989-304245 19890427; US 4953103 A US 1989-345397 19890428; EP 340972 A3 EP 1989-304245 19890427
PRAI JP 1988-105535 19880430
AB EP 340972 A UPAB: 19931118
The page **printer** with an internal **CPU** (15), interrupt controller (9), and direct memory access controller (DMAC) (18) has a direct memory access (DMA) **stopping circuit** (18a) in the DMAC the function of which is to stop DMA transfer in response to a DMA stop signal and **restart** it in response to a DMA **restart** signal. The DMA stop signal is generated by the interrupt controller (9) when it selects certain interrupt requests, such as communication interrupt requests, enabling the **CPU** (15) to service these requests promplty.

The DMA **restart** signal is generated at the end of the interrupt service routine. This arrangement permits MDA transfers to be performed in burst mode, stopping only when urgent interrupt service is required.

ADVANTAGE - Improves speed of operation of **printer**.

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L14 ANSWER 6 OF 18 JAPIO COPYRIGHT 2002 JPO
AN 1996-270608 JAPIO
TI CONTROL DEVICE FOR HYDRAULIC **CIRCUIT**
IN YAMADA KAZUHIKO
PA TOKAI RIKA CO LTD, JP (CO 000355)
PI JP 08270608 A 19961015 Heisei

AI JP1995-73668 (JP07073668 Heisei) 19950330
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 96, No. 10
AB PURPOSE: To provide a control device for a hydraulic **circuit** whereby supplying/ **stopping** operating oil can be performed by simple operation.
CONSTITUTION: A **reset** type switch is used in a turn inhibiting switch 4, to detect operation of this turn inhibiting switch 4 by a **CPU** 3. In the CPU3, a transistor 8 is alternately on/off controlled at each operating the turn inhibiting switch 4, to switch an upper turn unit to a turnable 'drive mode' and to an unturnable 'non-drive mode'. In the CPU3, a transistor 12 is on/off controlled at each operating the turn inhibiting switch 4, to put out an LED14 when switched to the 'drive mode' and to light the LED14 when switched to the 'non-drive mode'.

L14 ANSWER 7 OF 18 JAPIO COPYRIGHT 2002 JPO
AN 1995-107674 JAPIO
TI POWER SUPPLY CONTROLLING DEVICE
IN SUGITO YOJI; TAMURA NOBORU
PA CANON INC, JP (CO 000100)
PI JP 07107674 A 19950421 Heisei
AI JP1993-273226 (JP05273226 Heisei) 19931005
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No. 4
AB PURPOSE: To rationalize the control of the power supply of an electronic apparatus, which is driven with a battery, by turning OFF the power supply of the first electronic apparatus when the power supply of the first electronic apparatus, wherein the battery is the power supply, is in the ON state and the battery voltage has a value smaller than the specified value.
CONSTITUTION: In a interface part 10a on the side of a **printer**, the power supply voltage of a battery 21a is inputted into a power-supply driving **circuit** 20c when a power transistor 20b is turned ON with a switching transistor 20a, and the power is supplied into each part. The ON/OFF control signal of the switching transistor 20a is transferred from a interface 30a on the side of an electronic computer through a signal line 23a. When the battery voltage supplied from the power-supply driving **circuit** 20c becomes lower than the internal working voltage, a **CPU** 14 outputs the **reset** signal, and the supply of the battery voltage to each part from the power-supply driving **circuit** 20c is **stopped**. Thus the power supply control of the electronic apparatus such as the **printer** and the electronic computer driven by the battery 21a can be adequately performed.

L14 ANSWER 8 OF 18 JAPIO COPYRIGHT 2002 JPO
AN 1993-298127 JAPIO
TI FAULT INFORMATION PROTECTING SYSTEM FOR INFORMATION **PROCESSOR**
IN TATENO TAKESHI
PA NEC IBARAKI LTD, JP (CO 490946)
PI JP 05298127 A 19931112 Heisei
AI JP1992-121389 (JP04121389 Heisei) 19920415
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 1695, Vol. 18, No. 1, P. 113 (19940217)
AB PURPOSE: To prevent fault information from being destroyed by system **reset** after fault generation by providing a means to request the protection of the fault information and a means to request the forced stop of an information **processor** in response to this request.
CONSTITUTION: When a system **stop** request **circuit** 3 is started by a diagnostic **processor** 1, the system stop request to

forcedly stop a **CPU** 9 is transmitted to a system control **processor** 7. When the normal end of the system stop processing is informed from the system control **processor**, the diagnostic **processor** 1 activates a system **reset** suppressing request **circuit** 4 on the diagnostic **processor** 1 corresponding to a system **reset** instruction from a panel 5 for system control for preventing the fault information of the **CPU** 9 from being destroyed. When the system **reset** suppressing request is received, the system control **processor** 7 activates a system **reset** control signal suppression **circuit** 8 for suppressing system **reset** control signals and afterwards, only the signals to the control **processor** 7 are suppressed.

L14 ANSWER 9 OF 18 JAPIO COPYRIGHT 2002 JPO
AN 1990-001886 JAPIO
TI MULTICOLOR LASER BEAM **PRINTER**
IN KAWANA TAKASHI
PA CANON INC, JP (CO 000100)
PI JP 02001886 A 19900108 Heisei
AI JP1988-142764 (JP63142764 Heisei) 19880611
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 1021, Vol. 14, No. 136, P. 84 (19900314)
AB PURPOSE: To prevent the deterioration, flying off, fog, etc., of color toner unused for development in a developing means and to prevent the damage of a driving means by independently controlling the drive of each developing means based on the transmitting condition of each inputting color image signal.
CONSTITUTION: A set terminal S of a RSFF 21 (22) inputs a first color image signal 1a and second color image signal 1b. A **reset** terminal R inputs a top signal TOP from a hostocomputer 1. For instance, the signal 1a is transmitted to the terminal S of a **circuit** 21 in response to the rise of the top signal TOP; and when the signal 1b is not transmitted to the terminal S of a **circuit** 22 inspite of the rise of the top signal TOP, first and second image signal presence indicating signals Q1 and Q2 respectively turns into H and L. Based on this, a first motor driving **circuit** 16a is driven and a second motor driving **circuit** 16b is **stopped**, through the command of a **CPU** 12. When the terminals S of the **circuits** 21 and 22 inputs signals 1a and 1b, respectively, after the rise of the signal TOP, the **circuits** 16a and 16b are driven.

L14 ANSWER 10 OF 18 JAPIO COPYRIGHT 2002 JPO
AN 1989-161544 JAPIO
TI PROGRAM TRACING SYSTEM
IN MIZUGUCHI TADASHI
PA NEC CORP, JP (CO 000423)
PI JP 01161544 A 19890626 Heisei
AI JP1987-320675 (JP62320675 Heisei) 19871218
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 937, Vol. 13, No. 43, P. 11 (19890926)
AB PURPOSE: To confirm the running of a relevant routine and to quickly search the causes of runaway of a **processor**, system down, etc., at the time of debugging by storing in advance the addresses and instructions of the programs executed by a **CPU** by optional numbers.
CONSTITUTION: The program stored in a ROM/RAM 13 is formed as that, when a **CPU** 10 is **reset**, addresses and instruction information stored in a storing **circuit** 8 are read out by the quantity of 1,000 addresses and outputted to a **printer** 14. When the

CPU 10 runs away after executing an instruction while it runs a different routine, a monitoring **circuit** 11 outputs a storage stopping signal to a control **circuit** 9. The **circuit** 9 **stops** the writing control of addresses and instructions and the **CPU** 10 is **reset** by the monitoring **circuit** 11. Thereafter, the **CPU** 10 reads out the addresses and data stored in the **circuit** 8 in accordance with the instruction stored in the ROM/RAM 13 and outputs the addresses and data to the **printer** 14. Thus the **CPU** 10 can trace the program running state before the system down caused by the run away.

L14 ANSWER 11 OF 18 JAPIO COPYRIGHT 2002 JPO
AN 1988-270187 JAPIO
TI **PRINTER** DEVICE
IN OTA KOSAKU
PA TOSHIBA CORP, JP (CO 000307)
TOSHIBA COMPUT ENG CORP, JP (CO 486760)
PI JP 63270187 A 19881108 Showa
AI JP1987-106855 (JP62106855 Showa) 19870430
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 798, Vol. 13, No. 67, P. 143 (19890215)
AB PURPOSE: To enable a ribbon to be easily replaced without generating the deviation of printing position, by a method wherein, a carriage is brought to a stop so as to be movable in a width direction of a platen at the detection of the ribbon end of the film ribbon, and a printing position is stored so that the carriage can be returned to the printing position at the **restart** of the printing.
CONSTITUTION: Simultaneously with the start of printing, a film ribbon 21 is taken up by a taken up reel 24 while coming into slide contact with a sensor 18. At the time that a ribbon end part of the film ribbon 21 passes through the sensor 18 made of an electrode, the sensor 18 is electrically conducted to detect the ribbon end. With the detection of the ribbon end, a **CPU** 31 stops the exitation of a carriage motor 17 through a motor control **circuit** 37 to **stop** a carriage 15 in a movable condition and stores a printing position, which had been calculated in a printing position calculation **circuit** 37a of the control **circuit** 37, into a printing position storage area 34a of a RAM 34. After the stop of carriage motor 17 and the storage of the printing position are completed, a **printer** is set in a printing stop condition and, then, a ribbon replacement can be carried out.

L14 ANSWER 12 OF 18 JAPIO COPYRIGHT 2002 JPO
AN 1988-035375 JAPIO
TI PAGE NUMBER GENERATING SYSTEM
IN ITO SEIGO
PA TOSHIBA CORP, JP (CO 000307)
PI JP 63035375 A 19880216 Showa
AI JP1986-178812 (JP61178812 Showa) 19860731
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 717, Vol. 12, No. 247, P. 162 (19880713)
AB PURPOSE: To enable a document to be printed on both sides of a paper easily and speedily, by generating either odd page numbers or even page numbers in ascending order or descending order, and generating remaining page numbers in either ascending order or descending order after re-**resetting** papers.
CONSTITUTION: Where the last page number is an even number, an odd page number generating **circuit** 53 is started operating to serially outputting odd page numbers in ascending order to a last page number limiter 57. When the odd page number inputted to the limiter 57 does not

exceeds the last page number, the limiter 57 outputs the inputted odd page number to a page buffer developing device 7. A **printer** 4 finishes printing on all papers set, before the odd page number generated by the **circuit** 53 exceeds the last page number, and informs a printing controller 2 of the completion of printing through a page buffer document **printer** 3, upon which the printing controller 2 sends a control signal 800 to a flip-flop **circuit** 55, thereby **stopping** the operation of the **circuit** 53. Then, the operator re-sets all printed papers on the **printer** 4 in the state of being reversed upside down, upon which the printing controller 2 outputs the control signal 800 to the flip-flop **circuit** 55, thereby starting an even page number generating **circuit** 54.

L14 ANSWER 13 OF 18 JAPIO COPYRIGHT 2002 JPO
AN 1987-013374 JAPIO
TI **PRINTER**-CONTROLLING SYSTEM
IN NISHIOKA SATORU
PA FUJITSU LTD, JP (CO 000522)
PI JP 62013374 A 19870122 Showa
AI JP1985-152862 (JP60152862 Showa) 19850711
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 599, Vol. 11, No. 188, P. 15 (19870617)
AB PURPOSE: To ensure that a printing head is located in a home position region without fail when a printing command is subsequently issued and enable a rapid printing operation, by a system wherein when driving of a motor is stopped, the distance between that position and an estimated stopping position of the motor is calculated, and it is discriminated whether or not a carrier can be stopped in a home position region. CONSTITUTION: An end of printing is recognized by a printing area discriminating **circuit** 161 on the basis of a signal from a **CPU** 11, a counter 163 is **reset**, is started counting by a pulse from a pulse generator 162, and when driving of the motor 131f is stopped by the **CPU** 11, the counter 163 **stops** counting. The **circuit** 161 supplied with the count (corresponding to the period of time (t)) obtain the difference between the period of time (t) and a prestored time interval T by calculation, and when the difference is not more than a predetermined number of pulses, it is judged that the position of the carrier at the moment of stopping the motor 131f will lie in a printing region, and a predetermined signal is outputted to the **CPU** 11. The **CPU** 11 drives the motor 131f according to the signal, and stops driving the motor 131f at the time the carrier 131a is confirmed by a sensor 132b and is fed into the home position region.

L14 ANSWER 14 OF 18 JAPIO COPYRIGHT 2002 JPO
AN 1986-228553 JAPIO
TI DATA **PROCESSOR**
IN NINOMIYA YOSHIYUKI
PA RICOH CO LTD, JP (CO 000674)
PI JP 61228553 A 19861011 Showa
AI JP1985-69697 (JP60069697 Showa) 19850402
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 552, Vol. 11, No. 66, P. 77 (19870227)
AB PURPOSE: To attain the effective use of a data **processor** by providing a work/ work-**stop** control **circuit** and a gate **circuit** to a **printer** and using an internal **printer** and an external device as the serial ports for data communication. CONSTITUTION: A **printer** controller 2 receives data at a PRT-RD terminal from a microcomputer 1 after setting a PRT-OFF terminal at 'L'

(work) and discriminates whether the received data is equal to the request data for stop of working or not. When the received data is not equal to the request data, the received data is processed. While the PRT-OFF terminal is set at 'H' when said received data is equal to the working request data. Then it is discriminates whether the subsequent received data is equal to the working stop request data or not. When no coincidence is obtained between both data, the received data is neglected to perform no processing (working stop state). While the PRT-OFF terminal is **reset** to 'L' when the coincidence is obtained between said both data. Therefore the signal is delivered to outside from the computer 1 only when the controller 2 is inactive.

L14 ANSWER 15 OF 18 JAPIO COPYRIGHT 2002 JPO
AN 1986-208146 JAPIO
TI DETECTING **CIRCUIT** FOR **CPU** RUNAWAY
IN HIRASHIMA KUNIHIKO; TANAKA KAZUYUKI
PA SEIKO INSTR & ELECTRONICS LTD, JP (CO 000232)
PI JP 61208146 A 19860916 Showa
AI JP1985-48762 (JP60048762 Showa) 19850312
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 543, Vol. 11, No. 37, P. 129 (19870204)
AB PURPOSE: To eliminate limitations of a processing time for runaway detection by setting a flip-flop with a stationary clock signal, and initiating an interruption with said signal and **resetting** the flip-flop through software.
CONSTITUTION: A basic waveform generated by an oscillation **circuit** 4 is frequency-divided by a frequency dividing **circuit** 9 to obtain the stationary clock signal, which sets the flip-clip periodically. Said clock signal serves as an interruption signal 8 for a **CPU** 1, which **resets** the flip-flop 2 through software in this interruption processing. When the **CPU** 1 enters a runaway state, the flip-flop is not **reset**, so the flip-flop 2 is held set and the runaway is detected. Further, the fault stop of the oscillation **circuit** 4 is also detected by an oscillation **stop** detecting **circuit** 5 and its detection signal is applied to an OR gate 3, so the abnormality is detected.

L14 ANSWER 16 OF 18 JAPIO COPYRIGHT 2002 JPO
AN 1985-263235 JAPIO
TI MICROCOMPUTER SYSTEM
IN SHIYOUNAKA HISASHI
PA OMRON TATEISI ELECTRONICS CO, JP (CO 000294)
PI JP 60263235 A 19851226 Showa
AI JP1984-120583 (JP59120583 Showa) 19840612
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 459, Vol. 1, No. 143, P. 157 (19860527)
AB PURPOSE: To improve the reliability of an MCU system by applying an interruption to a microcomputer (MCU) from a timer **circuit**, when an abnormality is generated in a watch dog timer **circuit**, and generating an abnormality output to the outside from the MCU.
CONSTITUTION: A counting completion value of a counter 11 is set so as to be a little longer than one normal period of a clock for a watch dog timer. Accordingly, if an oscillating **circuit** 9 **stops**, or an oscillating period becomes long, a time-up is generated from the counter 11 before the counter 11 is **reset**, and an abnormality flag is set to a **processor** 2 by a time-up processing. As a result, in the main processing, an abnormality of its execution result is detected, an H output is generated from an outputting **circuit** 7, a light emitting diode 15 is driven through an NOR gate 14, and the

abnormality is informed to the inside. Also, this H output is supplied to a **reset** terminal RST of the **processor** 2, and **reset** forcibly.

L14 ANSWER 17 OF 18 JAPIO COPYRIGHT 2002 JPO
AN 1983-114980 JAPIO
TI PARER FEED CONTROL SYSTEM FOR **PRINTER**
IN KITANO SHIGERU
PA SHARP CORP, JP (CO 000504)
PI JP 58114980 A 19830708 Showa
AI JP1981-214625 (JP56214625 Showa) 19811228
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 246, Vol. 7, No. 2211, P. 108 (19830930)
AB PURPOSE: To shorten the time for controlling the paper feed by sending a high speed paper feed instruction to a print controller detecting the depression of a paper feeding key while a stop instruction is provided thereto with a host **CPU**.
CONSTITUTION: After the on-off state of a paper feeding key 4 is recognized with a host **CPU** 1 via an input **circuit** 5, the key 4 is depressed. The on-state is detected with the **CPU** 1 and a high speed paper feeding instruction code is fetched from a memory 3 and inputted into a **printer** controller 2 which sets a **printer** motor signal for a controlling flip flop (FF) 24 to be sent to a **printer** 6 through a terminal O2. At the same time, a memory element 29 is set to send a paper feeding signal to the **printer** 6 at a terminal O3 thereby executing the paper feed control. Then, after the release of depression in the key 4 is detected with the **CPU** 1 checking for the depression state of the key 4 via the **circuit** 5, a **stop** instruction code is fetched from the memory 3 to the controller 2 to **reset** the element 29, which turns off the paper feeding signal to stop the paper feeding control of the **printer** 6.

L14 ANSWER 18 OF 18 JAPIO COPYRIGHT 2002 JPO
AN 1981-014388 JAPIO
TI PRINT CONTROL SYSTEM
IN TAKEUCHI YUTAKA
PA CASIO COMPUT CO LTD, JP (CO 350750)
PI JP 56014388 A 19810212 Showa
AI JP1979-90027 (JP54090027 Showa) 19790716
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 59, Vol. 5, No. 641, P. 38 (19810430)
AB PURPOSE: To make a register only for comparison needless to simplify the **circuit**, by comparing one-digit components of print data and one-character components of reference data, which indicate the drum rotation position stored in a buffer, with each other in an adder **circuit** to obtain a print driving signal.
CONSTITUTION: In the print mode, the carry processing of adder **circuit** 22 is inhibited, and **circuit** 22 becomes the input enable state for timing pulses and **reset** pulses from the **printer**. When detecting the timing pulse, the **CPU** latches the caracter code of the first line of the print drum into latch **circuit** 23 from output line (d) of control part 11 and inputs it to input terminal (9) of **circuit** 22. Simultaneously, memory print character datas of the X register of RAM13 are read out successively to terminal (a) of **circuit** 22 and are compared with the character code of **circuit** 23, and the comparison result is written into shift register 50, and the print hammer is driven through output buffer 51 to perform printing for agreeing characters. When

printing is completed, the motor stop instruction is set from RAM14 to output signal control **circuit** 32 to **stop** motor driving, thus completing the print processing of one- line components.

L28 ANSWER 1 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 2000-447552 [39] WPIX
DNN N2000-334315
TI Opening-closing control apparatus for electrically driven shutter, has interlock release **circuit** which releases interlocking of shutter control panel when abnormality of control unit and operation is detected.
DC Q48 T06
PA (OMRO) OMRON KK
CYC 1
PI JP 2000160968 A 20000613 (200039)* 5p
ADT JP 2000160968 A JP 1998-337998 19981127
PRAI JP 1998-337998 19981127
AB JP2000160968 A UPAB: 20000818
NOVELTY - A shutter control panel operates a shutter by interlocking with control **signal** Dd' generated by a **central processing unit** (**CPU**) (10). Monitoring timer (11) converts **reset signal** (RS) into stop **signal** and **outputs** to **CPU** when abnormalities are detected in shutter operation and **CPU** and **stoppage** relay **circuit** (12) is operated immediately and releases interlocking by setting switching diode (15) in OFF state.
DETAILED DESCRIPTION - On detecting the running state of the **CPU**, the monitoring timer outputs a **reset signal** (RS) to the **CPU** and the shutter opening-closing is performed according to a control **signal** from the **CPU** by the shutter control panel, via a motor, interlocking with the control **signal** and the switching diode is set in the ON state. When accident lowering of shutter is indicated by a control **signal** Dd' the interlocking is released and the shutter is stopped. When abnormality is detected, the **reset signal** is converted into the stop **signal**.
USE - For opening-closing operation of shutter.
ADVANTAGE - Improves safety in operation by stopping descend of shutter by restricting abnormal operation.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the control apparatus.
CPU 10
Monitoring timer unit 11
Stoppage relay **circuit** 12
Switching diode 15
Dwg.2/3

L28 ANSWER 2 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 1997-462104 [43] WPIX
DNN N1997-384813
TI Control apparatus for production equipment e.g. injection moulding machine - has forced **stoppage circuit** that **stops** equipment based on second **reset signal**, input to **processor** during system abnormality.
DC T06 X25
PA (MATU) MATSUSHITA DENKI SANGYO KK
CYC 1
PI JP 09212201 A 19970815 (199743)* 6p
ADT JP 09212201 A JP 1996-14944 19960131
PRAI JP 1996-14944 19960131
AB JP 09212201 A UPAB: 19971030
The apparatus has a **processor** (1) which **outputs** a **signal** based on a predetermined program to control operation

condition of an equipment. An interface **circuit** (3) operates the equipment based on a control **signal** from the **processor** . The **processor** is **reset** during an abnormality generation such as hardware failure by a first **reset signal** output from a timer (2).

The **processor** is held in the **reset** state by a holding **circuit** (5). A forced **stoppage circuit** (6) performs **stoppage** of the **circuit** independent of the interface current based on a second **reset signal** input into a **reset** terminal of the **processor**.

ADVANTAGE - Prevents damage of **die** during system recovery movement.

Dwg.1/7

L28 ANSWER 3 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 1996-332570 [33] WPIX
TI Watchdog timer **circuit** - includes latch for instructing stop operation of watchdog according to **CPU**, comparator for comparing output of counter with **output** of **CPU** latch, and **reset circuit** for generating **reset signal** for **CPU**.
DC T01
IN KIM, D
PA (SMSU) SAMSUNG ELECTRONICS CO LTD
CYC 1
PI KR 9408853 B1 19940928 (199633)* 1p
ADT KR 9408853 B1 KR 1992-9197 19920528
PRAI KR 1992-9197 19920528
AB KR 9408853 B UPAB: 19960823
The watch dog timing **circuit** includes a first latch for instructing stop/operation of the watch dog timing according to the **output** of a **central processing unit**, a third latch for latching the **output** of the **central processing unit**, a NOR gate for deciding a watch dog cycle according to the initial **signal** of the **central processing unit** and the clear **signal** of the first latch, a counter for counting **signals** of a clock stage using the output of the NOR gate as a clear **signal**, a comparator for comparing the output of the counter with the output of the third latch, a **reset circuit** for generating a **reset signal** for **resetting** the **central processing unit**, and a second latch for generating a **reset** out **signal** of the **reset circuit** by latching the output of the comparator with a clock inverted by inverting the clock of the clock stage using an inverter.
Dwg.1/1

L28 ANSWER 4 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 1995-234650 [31] WPIX
DNN N1995-182936
TI Semiconductor **IC** for information **processor** e.g. portable computer, word **processor** - has flip-flop which holds output at power down mode of internal **circuit** for fixed time until **reset signal** is output from timer **circuit**.
DC T01 U22
PA (FUIT) FUJITSU LTD
CYC 1
PI JP 07141076 A 19950602 (199531)* 7p

ADT JP 07141076 A JP 1993-291072 19931119
PRAI JP 1993-291072 19931119
AB JP 07141076 A UPAB: 19950810
The semiconductor **IC** detects scram in a clock pulse (CLK) supplied to its external input terminal. When the scram occurs in the clock pulse, a flip-flop (13) holds the output at power down mode for an internal **circuit** (14). During this process, a clock **stop** detector **circuit** (11) outputs an active **signal** (S3).

The **signal** activates a timer (12) whose preset value is fixed. After the required count is computed, the timer outputs a **signal** (S5). The **signal** (S5) again **resets** the flip-flop, whose output is now changed back to normal state from power down state. The timer is **reset** back to normal position based on the output generated from the flip-flop.

ADVANTAGE - Simplifies switching circuitry of **IC**.

Dwg.1/4

=> D BIB AB 5-16

L28 ANSWER 5 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 1991-334419 [46] WPIX
CR 1997-079682 [08]
DNN N1991-256271
TI Photoelectric switching **circuit** with integrated counter and divider - generates light emission pulses with variable period and synchronised reading pulses for photodetector of reflected light.
DC S03 U21 W05
IN KAWAGUCHI, M; OI, K; SATOI, T
PA (IZUM) IDEC IZUMI CORP
CYC 4
PI EP 456482 A 19911113 (199146)*
R: DE FR GB
US 5099113 A 19920324 (199215) 24p
EP 456482 B1 19970409 (199719) EN 26p
R: DE FR GB
DE 69125522 E 19970515 (199725)
ADT EP 456482 A EP 1991-304150 19910508; US 5099113 A US 1991-697894 19910508; EP 456482 B1 EP 1991-304150 19910508; DE 69125522 E DE 1991-625522 19910508, EP 1991-304150 19910508
FDT DE 69125522 E Based on EP 456482
PRAI JP 1990-53390U 19900522; JP 1990-49440U 19900511; JP 1990-127668 19900516
AB EP 456482 A UPAB: 19971030
Object detection by pulse-modulated light (g1) involves a frequency divider consisting of D flip-flops (212-215) and an OR **circuit** (218) counting pulses of a reference clock (100). Reading pulses (g2) are produced for a photodetector (400) with a shift register **circuit**.

The OR **circuit** (218) **stops** the operation of the final stage (215) and starts the output from the holding **circuit** (520) to a **signal processor** (540) and **output** driver (560) for transmission of output **signal** through a switching transistor (208) to an external load (206).

ADVANTAGE - Cost is reduced with **circuits** having duplicate functions integrated, and output detection flip-flops eliminated. @(27pp Dwg.No.2/14)@

L28 ANSWER 6 OF 16 JAPIO COPYRIGHT 2002 JPO

AN 1997-218806 JAPIO
TI ABNORMALITY DETECTOR FOR CONTROL **CIRCUIT**
IN SUGANO TOMOAKI; ASAKURA MASAHIKO; ITO AKIRA; OKADA TADAYOSHI; SEN NAOHITO; FURUSAWA TORU; KAWAKURA TAKAYUKI; MORISHIMA YOSHIO
PA HONDA MOTOR CO LTD, JP (CO 000532)
MITSUBA CORP, JP (CO 351006)
PI JP 09218806 A 19970819 Heisei
AI JP1996-47995 (JP08047995 Heisei) 19960209
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 8
AB PURPOSE: TO BE SOLVED:To surely perform the abnormality detection of a control **circuit** by a simple configuration by comparing the count value set to a counter means and the count value stored in a memory before a counting is started and **resetting** the control **circuit** or **stopping** the output if the both values are different with each other.
CONSTITUTION: count initial value of a ROM 12 is set to a RAM 13 and the value is counted down according to the clock **signal** of a **CPU** 2. When the value becomes 0, a watch dog pulse is inputted in the check terminal CK of a watch dog timer 11 from the **CPU** 2. At this stage, the count initial value set to the RAM 13 as it is inputted in the comparison part 2b of the **CPU** 2 before the value is counted down. Also the count initial value of the ROM 12 is inputted in the comparison part 2b and the values are compared. If the values are not matched, the **CPU** 2 is made to performs a self-set. As a result, the watch dog timer 11 judges that the **CPU** 2 is abnormal, outputs an output stoppage **signal** to an output **circuit** 10 and **stops** the **output** from the **CPU** 2.

L28 ANSWER 8 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 1992-243088 JAPIO
TI REFRESH CONTROLLER
IN SAKAMOTO HIDEKI
PA MATSUSHITA ELECTRIC IND CO LTD, JP (CO 000582)
PI JP 04243088 A 19920831 Heisei
AI JP1991-4270 (JP03004270 Heisei) 19910118
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 1468, Vol. 17, No. 16, P. 59 (19930112)
AB PURPOSE: To provide the refresh controller which can refresh a dynamic random access memory with lower electric power consumption at the time of a resume mode.
CONSTITUTION: An auxiliary **CPU** 6 first **outputs** the resume **signal** via a **signal** line 14 to an auxiliary refresh control **circuit** 4 when a power switch 8 is turned off. The auxiliary refresh control **circuit** 4, then, outputs a **reset signal** via a **signal** line 15 to a main **CPU** 2 and a refresh control **circuit** 3. The main **CPU** 2 and the refresh control **circuit** 3 **stop** operating. A power source 7 is in succession turned off by the control of the auxiliary **CPU** 6, by which the supply of the power source to the main **CPU** 2 and the refresh control **circuit** 3 is shut off and the auxiliary **CPU** 6 starts a sleeve mode. The auxiliary refresh control **circuit** 4, thereafter, refreshes the dynamic random access memory 1 via a **signal** line 11 at a specified period in accordance with the clock outputted from a clock oscillator 5.

L28 ANSWER 9 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 1991-067316 JAPIO
TI CLOCK GENERATING **CIRCUIT**
IN MIO MASAO
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 03067316 A 19910322 Heisei
AI JP1989-203106 (JP01203106 Heisei) 19890805
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 1213, Vol. 15, No. 226, P. 112 (19910610)
AB PURPOSE: To miniaturize the constitution of a clock generating **circuit** by controlling a clock gate which supplies the input of an oscillation **circuit** to a **CPU** with the use of the output of an FF which uses the output of a comparator and the oscillation stop **signal** of the **CPU** as the set input and the **reset** input respectively.
CONSTITUTION: When an oscillation stop **signal** is received by an oscillation **circuit** 1 from a **CPU** 4, the oscillation of the **circuit** 1 is **stopped** and the FF 5 and 6 are **reset**. When an oscillation starting **signal** is supplied from outside, the FF 7 is set and a reference voltage generating **circuit** 6 inputs the reference voltage to a comparator 2. Simultaneously, the **CPU** 4 **outputs** a **signal** to oscillate the **circuit** 1. A ceramic or a crystal oscillator increases gradually its soscillation amplitude when the oscillation is started. When the maximum amplitude of oscillation is larger than that of the **circuit** 6, the comparator 2 outputs a **signal** to set the FF 5. Thus a buffer 3 is turned on to start the supply of clock to the **CPU** 4. Consequently, a programming operating is facilitated.

L28 ANSWER 10 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 1991-051928 JAPIO

TI SYSTEM **RESET CIRCUIT**
IN ODA AKIRA; HORI FUSAO
PA TOKYO ELECTRIC CO LTD, JP (CO 000356)
PI JP 03051928 A 19910306 Heisei
AI JP1989-186019 (JP01186019 Heisei) 19890720
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 1205, Vol. 15, No. 2, P. 100 (19910523)
AB PURPOSE: To surely **reset** an input/output port when the working of a **CPU** is interrupted by using a retriggerable single shot **circuit**.
CONSTITUTION: A **CPU** 21 **outputs** a .vphi. clock in its active state, and the output time of a high level **signal**, i.e., the desired output is decided for a retriggerable single shot **circuit** 33 based on a time constant secured between a capacitor 34 and a resistance 35. In this case, the output time is set longer than the cycle of the .vphi. clock. This .vphi. clock is stopped if the working of the **CPU** 21 is interrupted and therefore the transmission of the desired output is **stopped** from the **circuit** 33. Then an input/output port 24 is **reset**. As a result, the port 24 is surely **reset** when the **CPU** 21 is interrupted.

L28 ANSWER 11 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 1990-116953 JAPIO
TI INFORMATION **PROCESSOR**
IN AZUMA YOSHIYASU
PA NEC CORP, JP (CO 000423)
PI JP 02116953 A 19900501 Heisei
AI JP1988-269453 (JP63269453 Heisei) 19881027
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 1080, Vol. 14, No. 34, P. 95 (19900723)
AB PURPOSE: To exactly collect a state of each **processor** by constituting the title **processor** so that when a flag means shows that an operating instruction inputted from other **processor** is effective, the operation is executed in accordance with its operating instruction.
CONSTITUTION: When a diagnostic **processor outputs** a stop instruction to a **processor** 1, a clock control **circuit** 18 **stops** an output of a clock **signal** and the **processor** 1 stops its operation. Also, when a decoding **signal** of '1' is outputted to an AND **circuit** 24 of a **processor** 2 from a decoding **circuit** 11, a flag use FF 22 sets its output to effective '1', an output of the AND **circuit** 24 becomes effective '1', an FF 27 is **reset** through an OR 26 and its output is set to '0'. In accordance with its output, the operation of the **processor** 2 is stopped.

L28 ANSWER 12 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 1986-190637 JAPIO
TI AUTOMATIC **RESET** DEVICE AT COMPUTER TROUBLE
IN AKIYAMA KENJI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 61190637 A 19860825 Showa
AI JP1985-30274 (JP60030274 Showa) 19850220
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 536, Vol. 11, No. 15, P. 111 (19870116)
AB PURPOSE: To secure the reliability of a device and to improve the operating ratio by **resetting** an interface (I/F) **circuit** to **stop** the output to the external if troubles exceeding a prescription are detected in a certain time.

CONSTITUTION: When a trouble occurs in a CPU11, a self-diagnostic **circuit** 21 **resets** the CPU21, and contents of a counter **circuit** 22 are increased by +1. Though the CPU11 is **reset**, the output to an external device 3 is held as it is because an I/F **circuit** 12 is as it is, and the state of the external device 3 is held. The CPU11 is **restarted** after **reset**, the control is continued if any more trouble is not detected. When A-number of seconds elapses after the **restart** of the CPU11, a timer **circuit** 23 clears the counter **circuit** 22; but if a trouble is detected before the elapse of A-number of seconds, contents of the counter **circuit** 22 are increased by +1. At this time, it is judged that a serious trouble occurs in the **CPU**, and the **output signal** to the external is stopped to stop the external device 3.

L28 ANSWER 13 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 1986-098002 JAPIO
TI OSCILLATION DEVICE
IN AKEYAMA SHINICHIRO
PA NEC CORP, JP (CO 000423)
PI JP 61098002 A 19860516 Showa
AI JP1984-219011 (JP59219011 Showa) 19841018
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 438, Vol. 1, No. 275, P. 160 (19860918)
AB PURPOSE: To prevent completely the malfunction of an information **processor**, etc., due to the delay of the stopping operation of an oscillator by **resetting** a frequency divider simultaneously with the stop of oscillation based upon an oscillation stop **signal**.
CONSTITUTION: When the logical level of the oscillation stop **signal** 9 is low, the oscillation **circuit** 1 oscillates at a specific frequency, but when the logical level of the oscillation stop **signal** 9 is high, the oscillation **circuit** 1 **stops** oscillating and the frequency divider 2a is **reset** with the oscillation stop **signal** 9 and outputs a low-level **signal**. In this case, even if the oscillation of the oscillation **circuit** 1 does not stop completely, or if the time delay of the oscillation stop occurs, the supply of a clock **signal** to the information **processor** from the **output** 10 is stopped completely at desired timing by the **resetting** of the frequency divider 2a.

L28 ANSWER 14 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 1985-178975 JAPIO
TI **OUTPUT SIGNAL PROCESSOR** FOR ELECTROMAGNETIC PICKUP SENSOR
IN KOBAYASHI YASUHIRO
PA JAPAN ELECTRONIC CONTROL SYST CO LTD, JP (CO 470862)
PI JP 60178975 A 19850912 Showa
AI JP1984-34441 (JP59034441 Showa) 19840227
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 449, Vol. 1, No. 21, P. 15 (19860128)
AB PURPOSE: To detect zero-cross point of output **signal** accurately by providing a timer **circuit** for **stopping** function of a **signal** detection **circuit** until elasping predetermined time from starting time of transmission of a shaper **circuit**.
CONSTITUTION: A comparator 12 will produce a high **signal** until the output from an electromagnetic pickup sensor 11 will traverse the slice level from low to high. A timer **circuit** 14 will start function from the time point when the output from the comparator 12 has

changed from high to low and produce high **signal** at the **reset** terminal of flip-flop **circuit** 13 when the input **signal** has continued low for predetermined time. A rising detection **circuit** 15 will detect the zero- cross point of A.C. output **signal** from said sensor 11. In such a manner, erroneous detection of zero-cross point due to noise can be prevented.

L28 ANSWER 15 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 1984-144959 JAPIO
TI **RESET CIRCUIT**
IN HARUHARA FUSHIAKI; OBATA YOSHIHIRO
PA CHINO WORKS LTD, JP (CO 400125)
PI JP 59144959 A 19840820 Showa
AI JP1983-18696 (JP58018696 Showa) 19830207
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 322, Vol. 8, No. 2781, P. 97 (19841219)
AB PURPOSE: To obtain a highly safety **reset circuit** by **resetting** each **CPU** by a timer **circuit** without **stopping** the **CPU** immediately when abnormality is generated in the **CPU**, and when the **CPU** is **restarted** to continue its operation, but the abnormality is continued, stopping the whole **CPUs** by **outputs** from counters.
CONSTITUTION: Respective **CPUs** 11-13 **reset** respective timer **circuits** 21-23 at the time of normal operation to prevent the timer **circuits** from generating **signals**, but at the time of abnormality, the timer **circuits** 21-23 are not **reset** and supply instantaneous **reset** output **signals** such as pulses to the **CPUs** 11-13 through OR **circuits** 31-33 to **reset** and **restart** the **CPUs** 11-13. Counters 41, 42 count up **signals** from the timer **circuits** 21-23 by the prescribed number of times or more and supply output **signals** to a logical **circuit** 6 before being **reset** by timers and OR of respective outputs is latched by a latch **circuit** 7, so that the **CPUs** 11-13 are **reset** and the operation is stopped.

L28 ANSWER 16 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 1983-056042 JAPIO
TI PSEUDO PARITY ERROR GENEARATING **CIRCUIT** SYSTEM
IN TANIGUCHI TORU; TOMIZAWA SHINICHI; NAKAMURA SHIGERU
PA FUJITSU LTD, JP (CO 000522)
PI JP 58056042 A 19830402 Showa
AI JP1981-154973 (JP56154973 Showa) 19810930
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 205, Vol. 7, No. 1421, P. 109 (19830622)
AB PURPOSE: To make an error check without exerting any influence upon an original product by providing a pseudo parity error generating **circuit** to a common bus line connected with a microprocessor and an RAM.
CONSTITUTION: A **CPU outputs** a parity error processing program to a comparator 11 and a decoding **circuit** 12 through a bus 2. A prescribed address set with an address selection switch 10 is inputted to the comparator 11, whcih when those addresses coincide with each other, outputs a coincidence **signal** to an FF **circuit** 13 to output a **signal** 1 from the terminal Q. This **signal** is transmitted from a gate **circuit** 14 to the **CPU** as a constinuous parity error **signal** 9. On receiving this **signal**, the **CPU outputs** a

fixed pattern. This fixed pattern is inputted to the **circuit** 12, whose output **resets** the FF **circuit** 13 to **stop** the outputting of a **signal** 9. When the **CPU outputs** an end **signal**, the **circuit** 13 is **reset**.

=> D BIB AB 1-39

L35 ANSWER 1 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 2001-430746 [46] WPIX
TI Universal receiver capable of receiving satellite **signal** and the method thereof.
DC W02
IN LEE, W S
PA (EITE-N) EITECH
CYC 1
PI KR 2001001503 A 20010105 (200146)* 1p
ADT KR 2001001503 A KR 1999-20758 19990604
PRAI KR 1999-20758 19990604
AB KR2001001503 A UPAB: 20010815
NOVELTY - A universal receiver is provided to receive both ground wave and satellite broadcasting **signal** with a single **input** /output port, thereby realizing a simple hardware structure and decreasing manufacturing costs.
DETAILED DESCRIPTION - If a power switch is turned on, a micro control unit(MCU) supplies power to an analog processor, a digital **processor**, and an **output** circuit, and **initializes** a CPU(S1,S2). The CPU **initializes** the analog/the digital processors according to a control sequence of an execution program built in a program ROM(S3). The CPU refers to previous state information stored in an electrically erasable and programmable ROM(EEPROM) to control an output switch, and makes a cathode ray tube(CRT) display a previous power-on state channel(S4). The CPU supplies data for being displayed on a light emitting diode(**LED**) to the MCU. The MCU supplies the data to the **LED** to make the **LED** display a present mode state or channel information, and stands by until a user command is inputted(S5). If the user command is inputted, the command is supplied to the CPU by the MCU(S6). If the command is decided as a mode conversion command, the **CPU** controls the **output** switch to convert a present mode into a required mode(S7,S8). If the user command is a command except for the mode conversion command, the CPU maintains the present mode(S9). The CPU controls each unit to convert a channel according to the corresponding user command, and displays the converted channel or controls the volume(S10).
Dwg.1/10

L35 ANSWER 2 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 2001-377417 [40] WPIX
DNN N2001-276273
TI Information display system for use in point-of-sales system, has display units to simultaneously display image received from output unit via connector array.
DC P85 T01
PA (XERF) FUJI XEROX CO LTD
CYC 1
PI JP 2001066999 A 20010316 (200140)* 9p
ADT JP 2001066999 A JP 1999-241829 19990827
PRAI JP 1999-241829 19990827
AB JP2001066999 A UPAB: 20010719
NOVELTY - Image received from image **input** unit (1) is converted to display **format** by a **signal processor** (11) and **output** via output unit (12). Information for display is transmitted to display units (3-1 - 3-N) having memory function, and connected parallel to connector array (13). Image received in

input unit is displayed simultaneously in display units.
USE - For displaying information in output devices such as liquid crystal apparatus, CRT apparatus, recording devices such as OA apparatuses e.g. **printer**, copier, in point-of-sales system.
ADVANTAGE - Since several display units are provided with memory function, information can be displayed in all display units simultaneously. The display unit maintains display even without power supply, thus conserving energy. Size and weight are reduced and handling property is improved. Rewriting of information can be performed several times.
DESCRIPTION OF DRAWING(S) - The figure illustrates the block diagram of the display system. (The drawing includes non-English language text).
Image **input** unit 1
Display units 3-1 - 3-N
Signal processor 11
Output unit 12
Connector array 13
Dwg.1/9

L35 ANSWER 3 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 2001-171821 [18] WPIX
DNN N2001-124178
TI **Printer** for producing bank note, changes all image data to control **signals**, if accurate copy treatment command is **input** after completion of latent image **formation** on photoreceptor.
DC P75 T01 T04 W04
PA (SHIH) SEIKO EPSON CORP
CYC 1
PI JP 2000253239 A 20000914 (200118)* 8p
ADT JP 2000253239 A JP 1999-48566 19990225
PRAI JP 1999-48566 19990225
AB JP2000253239 A UPAB: 20010402
NOVELTY - Inaccurate copy treatment command is **input** to indicate existence of preset printing prohibition image in printing data and RAM (25) stores **input** image data. Control **signal** is **output** by **CPU** (22) to laser mechanism (34) that forms latent image on photoreceptor (33). If inaccurate copy treatment command is **input** after completion of latent image **formation**, all image data are changed to control **signals** by CPU.
DETAILED DESCRIPTION - If the inaccurate copy treatment command is not **input** after completion of latent image **formation**, the **CPU outputs** a control **signal** based on image data stored in RAM. An INDEPENDENT CLAIM is also included for printing system.
USE - For producing bank note.
ADVANTAGE - Since all image data are stored in RAM, incorrect copies of bank note is prevented.
DESCRIPTION OF DRAWING(S) - The figure shows circuit block diagram of **printer**.
CPU 22
RAM 25
Photoreceptor 33
Laser mechanism 34
Dwg.2/3

L35 ANSWER 4 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 2000-391732 [34] WPIX
DNN N2000-293628

TI Electronic device with CPU e.g. for copier, has gate circuit to cut-off **input-output signal** from **central processing unit** when stoppage of internal clock during sleep mode is detected by clock detection circuit.
DC S06 T01 T04 W02
PA (CANO) CANON KK; (COPY) COPYER KK
CYC 1
PI JP 2000132264 A 20000512 (200034)* 5p
ADT JP 2000132264 A JP 1998-316863 19981020
PRAI JP 1998-316863 19981020
AB JP2000132264 A UPAB: 20000718
NOVELTY - A central processing unit (CPU) (1) stops internal clock during sleep mode, whose stoppage is detected by a clock detection circuit (3). Based on the detected **signal**, **input**-output **signal** from the CPU is cut-off by a gate circuit (5) whereby the preset loads are made into OFF state. The internal clock of the CPU **restarts** an operation, when the sleep mode is released and the loads are switched ON.

USE - For stopping load operation and internal clock of copier, facsimile and **printer** during sleep mode.

ADVANTAGE - Generation of fault during sleep mode is prevented beforehand by providing the gate circuit.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of a copier with CPU.

Central processing unit 1
Clock detection circuit 3
Gate circuit 5
Dwg.1/4

L35 ANSWER 5 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 2000-089208 [08] WPIX
DNN N2000-070222
TI Converting print data **format** which converts a horizontal data **format** for printing N-byte data per line horizontally into a vertical data **format** for printing M-byte data vertically at a time.
DC T04 W02
IN KIM, W K; KIM, W G
PA (DAEW-N) DAEWOO TELECOM LTD; (DAEW-N) DAEWOO COMMUNICATIONS CO LTD
CYC 27
PI EP 967784 A2 19991229 (200008)* EN 28p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2000174972 A 20000623 (200036) 20p
KR 2000006435 A 20000125 (200063)
ADT EP 967784 A2 EP 1999-305013 19990625; JP 2000174972 A JP 1999-180903 19990625; KR 2000006435 A KR 1999-24083 19990624
PRAI KR 1998-24149 19980625
AB EP 967784 A UPAB: 20000215
NOVELTY - A DMA controller has a data **format** converter to generate vertical **format** data from horizontal **format** data.

DETAILED DESCRIPTION - The apparatus includes a data store with a first storing area where horizontal data are stored in sequence of the address and a second storing area where **format**-converted vertical data are stored. An address generator produces read address data to read K-byte data from the first storing area by adding a source address offset value to set read start address data. The value corresponds to the number of N. The generator produces write address data to write K-byte

data in the second storing area by adding a destination address offset value to set write start address data. The value corresponds to the number of M. The generator operates during on cycle of DMA operations. A DMA controller has a data **format** converter to generate K-byte data to be stored in the second storing area by grouping the K-byte data read from the data memory in the same bits. A timer sets the cycle of DMA operations, to output a bus request **signal** to CPU corresponding to a **signal** output from the timer and to execute the data **format** converting operations by controlling the address generator if a bus grant **signal** is **input** from **CPU**. A counter **outputs** an interrupt **signal** if the number of output times of the bus request **signal** from the DMA controller becomes M. A CPU registers the read start address data, write start address data, source address offset value and destination address offset value and controls the driving operations of the timer. An INDEPENDENT CLAIM is also given for an apparatus for converting print data that has ports to connect a data bus with an address bus.

USE - For converting print data from horizontal print data to vertical print data. For converting e.g. data for the thermal head of a facsimile machine to the vertical data **format** of an **ink jet** or **bubble jet printer**.

ADVANTAGE - Provides high speed data conversion in hardware by executing the converting operation using direct memory access, not affecting the processing speed of the CPU.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of the conversion apparatus.

Dwg.4/15

L35 ANSWER 6 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 2000-003795 [01] WPIX
DNN N2000-003241
TI Surge protection module for image forming apparatus like copier, **printer**, facsimile, etc - stops image forming operation when abnormality is detected in output value from A/D converter by CPU and then cuts off **input** from AC power supply using switch.
DC P84
PA (RICO) RICOH KK
CYC 1
PI JP 11282316 A 19991015 (200001)* 5p
ADT JP 11282316 A JP 1998-103521 19980331
PRAI JP 1998-103521 19980331
AB JP 11282316 A UPAB: 20000105

NOVELTY - When an abnormality is detected in the output value of an A/D converter (7e) by a CPU (7a) in a fixed time, a series of image forming operations are terminated and then a switch (1) cuts off the **input** from an AC power supply (8). DETAILED DESCRIPTION - An AC/DC converter (9) performs full wave rectification on the AC voltage supplied from the AC power supply and converts it to a DC voltage. The A/D converter converts the DC voltage supplied from the AC/DC converter to a digital **signal**. The CPU detects the abnormality in the output value from the A/D converter within a fixed time that can be changed.

USE - For protecting image forming apparatus like copier, **printer**, facsimile, etc from voltage surge.

ADVANTAGE - Prevents damage and malfunctioning of the image forming apparatus caused by the abnormal voltage reliably, as a series of image **formatting** operation gets terminated when abnormality is detected by the CPU and then the switch cuts off the **input** from the AC power supply. DESCRIPTION OF DRAWING(S) - The figure shows the circuit diagram of the copier. (1) Switch; (7a) CPU; (7e) A/D converter; (8) AC

power supply; (9) AC/DC converter.
Dwg.1/4

L35 ANSWER 7 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1998-605697 [51] WPIX
DNN N1998-472585
TI Image processor for e.g. colour facsimile machine - has CPU and buffer memory that **input** digital colour image **signal**, converted by CPU in same **format** as output of A-D converter, into image processing circuit which applies various image processings.
DC T01 W02
PA (BRER) BROTHER KOGYO KK
CYC 1
PI JP 10276322 A 19981013 (199851)* 6p
ADT JP 10276322 A JP 1997-80387 19970331
PRAI JP 1997-80387 19970331
AB JP 10276322 A UPAB: 19990113
The image processor has an A/D converter (22) that transforms an analogue colour image **signal** into a digital colour image **signal** based on the reflected light from a read document. An image processing circuit (26) applies various image processings to the converted digital colour image **signal**. An analogue switch (21) **inputs** another analogue colour image **signal** which has a different **format** compared with the analogue colour image **signal** fed into the A/D converter.

A CPU (1) converts the analogue colour image **signal** from the analogue switch into a digital colour image **signal** with a **format** similar to the output **signal** of the A/D converter. The CPU and a buffer memory (25) **input** the digital colour image **signal** from the CPU into the image processing circuit.

ADVANTAGE - Reduces manufacturing cost due to reduced number of image processings and components. Adds and processes video **printer** function even for standard colour TV **signals** e.g. NTSC system.
Dwg.2/2

L35 ANSWER 8 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1998-599087 [51] WPIX
DNN N1998-466477
TI High voltage power supply control system for image forming apparatus - includes AND gate which outputs **signal** to high voltage power supply, only when PWM **signal** and auxiliary **signal** are **input**.
DC P84 S06 T01 X12
PA (RICO) RICOH KK
CYC 1
PI JP 10268714 A 19981009 (199851)* 4p
ADT JP 10268714 A JP 1997-93089 19970327
PRAI JP 1997-93089 19970327
AB JP 10268714 A UPAB: 19981223
The system includes a timer (10) which sets a time at which a PWM **signal** is **output** from a **CPU** (200). The PWM **signal** is monitored by an IC (12) which outputs a **RESET signal**, after elapse of time set by timer. This **RESET signal** is **input** to another IC (13) which outputs an auxiliary **signal** of the PWM **signal**.

The PWM **signal** and the auxiliary **signal** are **input** to an AND gate (14) and the output from the AND gate is send to a high voltage power supply (100), only when both the PWM

signal and the auxiliary **signal** of PWM **signal** are **input** to the AND gate.
ADVANTAGE - Offers protection of high voltage power supply.
Dwg.1/3

L35 ANSWER 9 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1998-467126 [40] WPIX
DNN N1998-363957
TI Printing apparatus e.g. laser **printer** - has processor which modifies value of predetermined memory register to output transition in electrical **signal** directed to clear MSB **input** of counter.
DC P84 S06 T01 T04
IN OVERALL, G S; WADE, T C; WEBB, J F; WRIGHT, P B
PA (LEXM-N) LEXMARK INT INC
CYC 30
PI US 5797061 A 19980818 (199840)* 27p
EP 878745 A2 19981118 (199850) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
CN 1199184 A 19981118 (199914)
JP 11095960 A 19990409 (199925) 87p
KR 98086927 A 19981205 (200009)
TW 410279 A 20001101 (200117)
ADT US 5797061 A US 1997-854875 19970512; EP 878745 A2 EP 1998-108603 19980512; CN 1199184 A CN 1998-108310 19980512; JP 11095960 A JP 1998-169101 19980512; KR 98086927 A KR 1998-16770 19980511; TW 410279 A TW 1998-107337 19980718
PRAI US 1997-854875 19970512
AB US 5797061 A UPAB: 19981008
The apparatus (10) has a printing unit which comprises an electrical circuit for sending print data in a serial **format** as a first electrical **signal** to a print head. A second electrical **signal** is also transmitted to a counter having an MSB output that produces and directs a third electrical **signal** to a processor. The counter also has a clear MSB **input** that receives a fourth electrical **signal output** by the **processor**.
The MSB output remains at a first logic state until counter accumulates enough count value and then it is changed to a second logic state. The processor modifies the value of a predetermined memory to output a transition in fourth electrical **signal** directed to clear MSB **input** of counter. The MSB output is thus cleared to first logic state. The counter continues to accumulate count value at its other count outputs.
ADVANTAGE - Improves updating capability of remaining toner usage prediction.
Dwg.1/7

L35 ANSWER 10 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1998-421851 [36] WPIX
DNN N1998-329433
TI Image recording control apparatus - has **CPU** to acknowledge **output** of command and based on mode switching **signal** generated by **signal** generator.
DC P75 S06 T01
PA (CANO) CANON KK
CYC 1
PI JP 10175355 A 19980630 (199836)* 20p
ADT JP 10175355 A JP 1997-279027 19971013

PRAI JP 1996-275851 19961018
AB JP 10175355 A UPAB: 19980911
The apparatus has an image **signal** processor (20) which generates an image data. The image **signal** processor also analyses the **input** to an image **formation** unit. The image **formation** unit is controlled by an image **formation** control unit (12) based on the first command from the image **signal** processor and image is formed on a recording medium.

The operation of the image **formation** unit is checked by another command from a control unit. The check mode is indicated by a mode switching **signal** which is generated by a **signal** generator. Based on the mode switching **signal**, a switch (22) is operated to replace first command **signal** by second command **signal**. The acknowledgement of second command is done by a CPU (13,21).

ADVANTAGE - Prevents switching to check mode when mode switching **signal** is not generated.
Dwg.2/16

L35 ANSWER 11 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1997-255060 [23] WPIX
DNN N1997-211215
TI Image forming appts such as copier, **printer**, facsimile - includes reverse sending sheet detector which generates detection **signal input** to **CPU** which **outputs** conversion operation **signal** to spur roller and discharge roller.
DC P75 Q36 S06 T04 W02
PA (CANO) CANON KK
CYC 1
PI JP 09086756 A 19970331 (199723)* 11p
ADT JP 09086756 A JP 1995-244830 19950922
PRAI JP 1995-244830 19950922
AB JP 09086756 A UPAB: 19970606
The appts (1) consists of a platen roller (18) which feeds the sheet from a sheet loading plate (16). The sheet is subjected to U turn by an U turn guide (20) and an **ink jet** head (22) forms an image on the sheet. A spur roller (23) and discharge roller (24) conveys the sheet through a discharge opening (60).

A reverse sending sheet detector (29) generates detection **signal** of the sheet supplied from discharge opening. The detection **signal** is **input** to a CPU (50). The CPU **inputs** an inversion operation **signal** to spur roller and discharge roller. The reversed sheet is conveyed from discharge opening to a sheet guide (31) arranged between U turn guide and **ink jet** head.

ADVANTAGE - Forms image on thick sheet easily. Improves operativity. Performs accurate and reliable image **formation** on sheet.
Dwg.1/8

L35 ANSWER 12 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1997-149278 [14] WPIX
DNN N1997-123335
TI Recording device e.g. inkjet type **printer** - outputs acknowledge **signal** to computer when second timer is started and is then made inactive after third timer, after predetermined time lapse.
DC P75 T01 T04
PA (BRER) BROTHER KOGYO KK
CYC 1
PI JP 09024659 A 19970128 (199714)* 10p

ADT JP 09024659 A JP 1995-175812 19950712
PRAI JP 1995-175812 19950712
AB JP 09024659 A UPAB: 19970407
The device receives data from a host computer (4) which is then latched in a data register (22). A flip flop (24) is set based on the strobe **signal** received from the computer. An interruption **signal** is **input** into a CPU (6) which reads the latched data. The data is then printed based on the **output** of the **CPU**. The state of the flip flop (30) is inverted and a busy **signal** is output to the computer. When the CPU has finalized its reading operation, the flip flop is **reset**.

A first timer (A) is started and after the predetermined time, the busy **signal** is made non-active. The second and third timers (B,C) are started. When the second timer is started, an acknowledge **signal** is output to the computer. The acknowledge **signal** is made non-active after predetermined time after the operation of the third timer.

ADVANTAGE - Facilitates alteration of time. Performs handshaking operation without using CPU. Increases resolution.
Dwg.2/5

L35 ANSWER 13 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1996-135817 [14] WPIX
DNN N1996-114346
TI Image forming appts. e.g. **printer** or facsimile - has tray assigned to carry accommodation storage of recording medium output based on memory data table when image **formation** demand generates controller.
DC P75 P84 Q36 S06 T04 W02
PA (CANO) CANON KK
CYC 1
PI JP 08026586 A 19960130 (199614)* 18p
ADT JP 08026586 A JP 1994-166835 19940719
PRAI JP 1994-166835 19940719
AB JP 08026586 A UPAB: 19960417
The appts. has an image-**signal input** unit that **inputs** several image **signals** which is then processed in an image-**signal** processing unit in a state that carries out an image **formation**. The output of the image-**signal** processing component passes an image **formation** unit which carries out the image **formation** at a recording medium. An **output processor** for the recording medium provides several stored trays.

A memory unit stores the assignment state of each tray as a data table. The stored tray has a tray change unit for changing the conveyance path so that the recording medium will correspond to an assigned tray. The recording medium storage situation of each tray is detected by a detector and then displayed in a display unit. A controller controls the operation of each unit.

ADVANTAGE - Provides effective sorter output bin and reduces time for looking delivery position.
Dwg.1/14

L35 ANSWER 14 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1994-298356 [37] WPIX
CR 1994-308586 [38]
DNN N1994-234940
TI Image **formation** device eg. for **printer** - has pulse width modulator **processor** which **outputs signal**

to laser driver in which sensitivity drum is exposed according to **input** data NoAbstract.
DC T01 T04 W02
PA (CANO) CANON KK
CYC 1
PI JP 06225128 A 19940812 (199437)* 40p
ADT JP 06225128 A JP 1993-12677 19930128
PRAI JP 1993-12677 19930128
AB JP 06225128 A UPAB: 19960305
Dwg.1/51

L35 ANSWER 15 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1994-216145 [26] WPIX
DNN N1994-170697
TI Data processor for computer engineering - has data **inputs**-**outputs** of first **processor** connected to data **inputs**-outputs of first RAM.
DC T01
IN CHURAKOV, V L; KREMNEV, A V; SHAKHOV, A N
PA (CHUR-I) CHURAKOV V L
CYC 1
PI SU 1810892 A1 19930423 (199426)* 11p
ADT SU 1810892 A1 SU 1989-4629333 19890102
PRAI SU 1989-4629333 19890102
AB SU 1810892 A UPAB: 19940817
The data processor incorporates a data **formation** device (1), a control **signal** shaper (2), an address former (3), a priority unit (5), a first processor (6), RAMs (4,9,13), ROMs (7,8,14), a two-port RAM (10), a second processor (12), inputting (16) and outputting (15) units, a display panel interface (17), a display panel (18), a **printer** interface (19), and a **printer** (20). An **input** data accompanied by a sync. **signal** arrives at the **input** of the data **formation** device (1).
USE/ADVANTAGE - For designing control and data gathering systems. Higher speed of response. Bul.15/23.4.93
Dwg.1/9

L35 ANSWER 16 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1994-035261 [04] WPIX
CR 1998-311831 [27]; 2000-586033 [41]
DNN N1994-027392
TI Single chip IC appts. for video instruction set computing - has functional units to handle communication, bandwidth adaption, application control, multimedia management and universal video encoding.
DC T01 U13 W04
IN SHAW, S M; SHAW, V M
PA (SHAW-I) SHAW S M; (SHAW-I) SHAW V M
CYC 37
PI WO 9401824 A1 19940120 (199404)* EN 116p
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL OA PT SE
W: AT AU BB BG BR CA CH DE DK ES FI GB HU JP KP KR LK LU MG MN MW NL NO PL RO RU SD SE US
AU 9347686 A 19940131 (199422)
GB 2284525 A 19950607 (199526) 1p
US 5457780 A 19951010 (199546) 17p
GB 2284525 B 19960320 (199615) 1p
US 5611038 A 19970311 (199716)# 86p
AU 677791 B 19970508 (199727)
CA 2139660 C 20000314 (200032) EN

ADT WO 9401824 A1 WO 1993-US5863 19930617; AU 9347686 A AU 1993-47686 19930617; GB 2284525 A WO 1993-US5863 19930617, GB 1995-137 19950105; US 5457780 A CIP of US 1991-686773 19910417, US 1992-909312 19920706; GB 2284525 B WO 1993-US5863 19930617, GB 1995-137 19950105; US 5611038 A Cont of US 1991-686773 19910417, US 1994-297409 19940829; AU 677791 B AU 1993-47686 19930617; CA 2139660 C CA 1993-2139660 19930617, WO 1993-US5863 19930617

FDT AU 9347686 A Based on WO 9401824; GB 2284525 A Based on WO 9401824; GB 2284525 B Based on WO 9401824; AU 677791 B Previous Publ. AU 9347686, Based on WO 9401824; CA 2139660 C Based on WO 9401824

PRAI US 1992-909312 19920706; US 1991-686773 19910417; US 1994-297409 19940829

AB WO 9401824 A UPAB: 20001106
The single chip integrated circuit system includes functional units based on Video-Instruction-Set-Computing(VISC). The chip includes a number of functional units. A scalable **formatter** element handles arbitrary external video **formats** and adapt to internal **formats** accounting for available bandwidth. Video data blocks are held in a smart memory. The circuit also has an embedded RISC or CISC co-processor element to support DOS etc.

Using a real-time object-oriented operating system with concurrent execution of application and VISC the unit provides processing for interactive video, HDTV and multimedia communications.

ADVANTAGE - Provides a scalable integrated computing architecture for digital or algorithmic complex data types.

Dwg.1/4

L35 ANSWER 17 OF 39 WPIX (C) 2002 THOMSON DERWENT

AN 1993-046936 [06] WPIX

DNN N1993-035955

TI Protection system for critical computer memory information - has latch and window circuits for selectively coupling write strobe **output** of **processor** to memory after processor sets and clears latched **signal**.

DC T01 T05

IN AEBI, T; WICHT, P; AEBL, T

PA (ASCO-N) ASCOM AUTELCA AG; (ASCO-N) ASCOM HASLER AG; (ASCO-N) ASCOM HASLER MAILING SYSTEMS AG; (ASCO-N) ASCOM HASLER MAILING SYSTEMS INC; (ASCO-N) ASCOM AUTELCA LTD

CYC 16

PI EP 527010 A2 19930210 (199306)* EN 10p
R: AT BE CH DE DK ES FR GB IT LI NL PT SE
CA 2072504 A 19930206 (199331)
US 5276844 A 19940104 (199402) 10p
EP 527010 A3 19931118 (199512)
EP 527010 B1 19960424 (199621) EN 13p
R: AT BE CH DE DK ES FR GB IT LI NL PT SE
DE 69210135 E 19960530 (199627)
SG 49193 A1 19980518 (199835)

ADT EP 527010 A2 EP 1992-306830 19920727; CA 2072504 A CA 1992-2072504 19920626; US 5276844 A US 1991-740427 19910805; EP 527010 B1 EP 1992-306830 19920727; DE 69210135 E DE 1992-610135 19920727, EP 1992-306830 19920727; SG 49193 A1 SG 1996-7456 19920727

FDT DE 69210135 E Based on EP 527010

PRAI US 1991-740427 19910805

AB EP 527010 A UPAB: 19950705
The computer system includes a processor (10) having a write strobe output (15) and address outputs operable to execute a stored program. The system also has a memory (11,12,13), an address decoder (16), and a window

circuit (70). Typically the first memory is an EEPROM and the other two are battery-backed-up CMOS RAM.

The window circuit has a latch (80) which selectively couples the write strobe output (15) of the processor with the write strobe **input** of the memory in response to the processor's setting and clearing of a latched **signal**. A counter **resets** the processor if the latched **signal** is set and not cleared within a predetermined time period.

USE/ADVANTAGE - For postage meter etc. Increased protection of data against loss caused by faults and processor malfunction.

4/5

Dwg.4/5

L35 ANSWER 18 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1990-241234 [32] WPIX
DNN N1990-187191
TI Computer output device detecting pattern on preprinted **input** paper - detects coded marks indicating nature of form and prints item in required **format**.
DC P75 T04
IN MONRO, P
PA (HAMP-N) HAMPSHIRE ADVISORY
CYC 1
PI GB 2227718 A 19900808 (199032)*
ADT GB 2227718 A GB 1988-272869 19881122
PRAI GB 1988-27286 19881122; GB 1988-272869 19881122
AB GB 2227718 A UPAB: 19930928
The selective **printer** fills in preprinted forms. It is controlled in association with a sensor which detects coded marks on the form stock. The **format** and content of the selectively printed matter are adapted to the nature of the selected form. The form stock includes a variety of different successive forms, each identified by a code mark. The **printer** searches for the particular form required for an item, prints the item in the **format** dictated by the form, and then cancels the code mark on the filled form.

Signals characterising the mark are sent to a data **processor** which **outputs** an appropriate data file. It inhibits output of incorrect data files and avoids overprinting.

ADVANTAGE - Enables a number of different but related documents to be prepared without either a number of machines or a change of form stock.

1/3

L35 ANSWER 19 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1988-106344 [16] WPIX
DNN N1988-080663
TI **Signal** processor for resistance bridge output in weighing appts. - uses amplifier and voltage-frequency converter using reference **signal** obtained from bridge-supply.
DC S01 S02
IN BAUSCH, M; SCHNEIDER, G
PA (ENDR) ENDRESS & HAUSER GMBH & CO
CYC 4
PI DE 3633790 A 19880414 (198816)* 10p
GB 2196131 A 19880420 (198816)
FR 2604792 A 19880408 (198821)
DE 3633790 C 19890105 (198902)
US 4862382 A 19890829 (198944) 38p
GB 2196131 B 19910327 (199113)
ADT DE 3633790 A DE 1986-3633790 19861003; GB 2196131 A GB 1987-23296

19871005; US 4862382 A US 1989-25537 19890829
PRAI DE 1986-3633790 19861003
AB DE 3633790 A UPAB: 19930923
The **signal** processing stage uses a bridge amplifier (19) and a voltage/frequency converter (25) with **signal** and reference **inputs** (21,22; 20,23). The DC or AC voltage (Uv) fed to the bridge (13..16) has a switched polarity, with the momentary supply voltage (Uv) used as the reference for the voltage/frequency converter (25).

The polarity switching of the bridge supply voltage (Uv) is synchronised with the output **signal** frequency of the voltage/frequency coverter (25). The frequency measurement of the output **signal** provided by the **signal** processing stage is effected by a subsequent evaluation stage with a mean value obtained for a number of successive switching periods.

USE - For precision weighing appts.

1/4

L35 ANSWER 20 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1984-232256 [38] WPIX
CR 1984-232231 [38]
DNN N1984-173693
TI Colour control suitable for **ink jet printer** - selects densities of ink and with yellow concn. lowest for accurate flesh tone rendition.
DC P75 P84 S06 T04
IN KAWAMURA, H; SAKURADA, N; SASAKI, T
PA (CANO) CANON KK
CYC 5
PI DE 3408545 A 19840913 (198438)* 46p
FR 2542256 A 19840914 (198442)
JP 59163964 A 19840917 (198443)
GB 2139450 A 19841107 (198445)
GB 2139450 B 19871216 (198750)
DE 3448359 A 19891130 (198949)
DE 3408545 C 19900726 (199030)
US 4959659 A 19900925 (199041)
DE 3448359 C2 19950817 (199537) 16p
ADT DE 3408545 A DE 1984-3408545 19840308; JP 59163964 A JP 1983-37698 19830308; GB 2139450 A GB 1984-5773 19840306; DE 3448359 A DE 1984-3448359 19840308; US 4959659 A US 1988-212097 19880627; DE 3448359 C2 Div ex DE 1984-3408545 19840308, DE 1984-3448359 19840308
FDT DE 3448359 C2 Div ex DE 3408545
PRAI JP 1983-75857 19830428; JP 1983-37698 19830308
AB DE 3408545 A UPAB: 19950927
The colour printing process uses an **ink jet** array with each colour having a choice of two jets, each with different colour densities. This provides a wide range of colour effects without affecting the picture quality and resolution.

The density of the yellow ink is always lower than that of the magenta and cyan so that flesh tones can be accurately reproduced.

0/17
Dwg.0/17

L35 ANSWER 21 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1984-232233 [38] WPIX
DNN N1984-173672
TI System processing picture data - comprises mixed-data serial transfer device, separator and processor to reproduce image.
DC P84 S06 W02

IN ABE, S; KAWAMURA, N
PA (CANO) CANON KK
CYC 5
PI DE 3408334 A 19840913 (198438)* 32p
JP 59163965 A 19840917 (198443)
GB 2139451 A 19841107 (198445)
GB 2139451 B 19870923 (198738)
US 4713684 A 19871215 (198806)
DE 3448411 A 19910307 (199111)
DE 3408334 C 19911205 (199149)
DE 3448411 C2 19940825 (199432) 19p
ADT DE 3408334 A DE 1984-3408334 19840307; JP 59163965 A JP 1983-37707 19830308; GB 2139451 A GB 1984-6070 19840308; US 4713684 A US 1987-39762 19870417; DE 3448411 A DE 1984-3448411 19840307; DE 3448411 C2 Div ex DE 1984-3408334 19840307, DE 1984-3448411 19840307
FDT DE 3448411 C2 Div ex DE 3408334
PRAI JP 1983-37707 19830308
AB DE 3408334 A UPAB: 19930925
In the system the data may be received by telephone line or other remote transfer device. Data of various types are transferred by a host computer (10) in series to the digital **printer** (8). The **printer** incorporates a separator (1), which separates the incoming data into blue (B), green (G), and red (R) **signals**.

These are fed to a picture **signal** processing circuit (2), which feeds its output to four memory stores (3,4,5,6), one of which relates to yellow (3), one to magenta (4), one to Prussian blue (5) and one to black (6). A four drum laser **printer** (7) forms an image on each of the four drums, which is composed of the respective colour dots and each drum in turn transfers its colour image to the same piece of paper to produce the final picture.

USE - For processing picture data e.g. in a digital colour copying machine.

1/11

L35 ANSWER 22 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1983-H5985K [23] WPIX
DNN N1983-098724
TI Oscilloscope probe calibration judging method - uses CPU to process comparison of output with reference level according to duty factor of square wave **signal**.
DC S01
IN FUKUTA, M; MANOME, T; MIKI, Y; TAKIT, K
PA (SONY) SONY TEKTRONIX CORP
CYC 5
PI GB 2109945 A 19830608 (198323)* 29p
FR 2516661 A 19830520 (198325)
DE 3242441 A 19830630 (198327)
CA 1203283 A 19860415 (198619)
GB 2109945 B 19860529 (198622)
US 4608657 A 19860826 (198637)
DE 3242441 C 19911114 (199146)
ADT GB 2109945 A GB 1982-31895 19821109; US 4608657 A US 1982-438101 19821101
PRAI JP 1981-184095 19811117
AB GB 2109945 A UPAB: 19930925
A square-wave **signal** is applied to a probe to be judged and a reference level is judged to be equal to a peak level of an output **signal** from the probe. The reference level is compared with the output **signal** from the probe and the probe is judged to be calibrated when the duty factors of the comparison result and the

square-wave **signal** are equal to each another. The reference level is adjusted to a level slightly lower than the max. peak level of the output **signal** of the probe or alternatively to a level slightly higher than the minimum peak level of the output **signal** . The result of the comparison and judgement steps may be displayed. 1/10

L35 ANSWER 23 OF 39 WPIX (C) 2002 THOMSON DERWENT
AN 1982-F7809E [20] WPIX
CR 1982-A2572E [02]; 1985-020873 [04]; 1985-033337 [06]; 1985-089024 [15]; 1985-130245 [22]; 1985-130246 [22]; 1985-154865 [26]; 1985-225323 [37]
TI Serial **printer** with sentence memory - has subtraction memory preset to predetermined valve, stepwise decreased and which stops corresponding drive upon arrival at preset value.
DC P75 P85 T01 T04
IN KONDO, H; NAKAJIMA, H; OZAWA, T; UEDA, H; YAMADA, Y; NAKAIJIMA, H
PA (CANO) CANON KK
CYC 11
PI

GB 2087115	A	19820519 (198220)*		69p
DE 3153020	A	19830901 (198336)		
ES 8307596	A	19831101 (198406)		
AU 8320472	A	19840216 (198414)		
AU 8425179	A	19840614 (198431)		
CA 1181711	A	19850129 (198509)		
DE 3153241	A	19850509 (198520)		
AU 8538209	A	19850530 (198529)		
SE 8502077	A	19850429 (198540)		
GB 2087115	B	19851009 (198541)		
FR 2561585	A	19850927 (198545)		
US 4558965	A	19851217 (198602)		
US 4615631	A	19861007 (198643)		
NL 8700163	A	19870504 (198722)		
CH 662533	A	19871015 (198746)		
CH 662784	A	19871030 (198746)		
US 4725158	A	19880216 (198810)		
US 4735515	A	19880405 (198816)		
SE 456234	B	19880919 (198840)		
DE 3153020	C	19881013 (198841)		
DE 3143138	C	19890524 (198921)		
US 4846593	A	19890711 (198935)		
US 4880325	A	19891114 (199004)		
DE 3153729	A	19910221 (199109)		
DE 3153727	A	19910228 (199110)		
IT 1197425	B	19881130 (199112)		
DE 3153728	A	19910321 (199113)		
DE 3153241	C	19910718 (199129)		
US 5037223	A	19910806 (199134)		
US 5108203	A	19920428 (199220)		68p
SE 467654	B	19920824 (199237)		
US 5322376	A	19940621 (199424)		70p
US 5484214	A	19960116 (199609)		68p
US 5529406	A	19960625 (199631)		68p
US 5562355	A	19961008 (199646)		67p
DE 3153729	C2	19970507 (199723)		29p
US 5690435	A	19971125 (199802)		
NL 192977	B	19980302 (199813)		35p

ADT GB 2087115 A GB 1981-32605 19811029; DE 3153020 A DE 1981-3153241 19811030; DE 3153241 A DE 1981-3153020 19811030; US 4558965 A US 1985-695760 19850129; US 4615631 A US 1984-642737 19840820; US 4725158 A

US 1987-9090 19870127; US 4735515 A US 1986-821132 19860122; DE 3153020 C DE 1981-3143138 19811030; US 4846593 A US 1988-150493 19880201; US 4880325 A US 1987-4271 19870106; DE 3153729 A DE 1981-3153729 19811030; DE 3153728 A DE 1981-3153728 19811030; US 5037223 A US 1989-442418 19891122; US 5108203 A US 1991-641631 19910117; SE 467654 B SE 1981-6390 19811029; US 5322376 A Cont of US 1981-314441 19811023, Cont of US 1984-664945 19841026, Cont of US 1986-883447 19860710, Cont of US 1987-63781 19870622, Cont of US 1988-230677 19880808, US 1990-627919 19901217; US 5484214 A Cont of US 1981-314441 19811023, Cont of US 1984-664945 19841026, Cont of US 1986-883447 19860710, Cont of US 1987-63781 19870622, Cont of US 1988-230677 19880808, Div ex US 1990-627919 19901217, US 1992-906678 19920630; US 5529406 A Cont of US 1981-314441 19811023, Cont of US 1984-664945 19841026, Cont of US 1986-883447 19860710, Cont of US 1987-63781 19870622, Cont of US 1988-230677 19880808, Div ex US 1990-627919 19901217, Div ex US 1992-906678 19920630, US 1994-297837 19940830; US 5562355 A Cont of US 1981-314441 19811023, Cont of US 1984-664945 19841026, Cont of US 1986-883447 19860710, Cont of US 1987-63781 19870622, Cont of US 1988-230677 19880808, Div ex US 1990-627919 19901217, Cont of US 1992-906663 19920630, US 1994-235230 19940429; DE 3153729 C2 Div ex DE 1981-3153241 19811030, DE 1981-3153729 19811030; US 5690435 A Cont of US 1981-314441 19811023, Cont of US 1984-664945 19841026, Cont of US 1986-883447 19860710, Cont of US 1987-63781 19870622, Cont of US 1988-230677 19880808, Div ex US 1990-627919 19901217, Cont of US 1992-906672 19920630, US 1994-193671 19940208; NL 192977 B NL 1981-4942 19811030

FDT US 5484214 A Div ex US 5322376; US 5529406 A Cont of US 4940063, Div ex US 5322376; US 5562355 A Div ex US 5322376; DE 3153729 C2 Div ex DE 3153241; US 5690435 A Div ex US 5322376

PRAI JP 1980-166635 19801128; JP 1980-152103 19801031; JP 1980-152104 19801031; JP 1980-152105 19801031; JP 1980-152106 19801031; JP 1980-160692 19801117; JP 1980-160693 19801117; JP 1980-160694 19801117; JP 1980-164527 19801125; JP 1980-164530 19801125

AB GB 2087115 A UPAB: 19980323

The electronic typewriter with a carriage supporting a front wheel, has a sentence memory and display, for word processing. A print pressure table controls hammer duration (using a counter) depending on the character size, for uniform print density. A print pitch table controls print pitch, and ribbon feed (using a counter), according to character width. The front wheel can be exchanged according to character size/pitch, the table outputs being multiplied by coefficients depending on the wheel to reduce memory size. Feedback through an RC circuit is used near the target position in positioning the front wheel, and also the carriage.

Carriage position is indicated on one of three scales according to pitch selected. Sheet feed can be controlled (using a counter) from the keyboard, via the sentence memory. A counter can scan the keys, a two bit latch corresponding to an actuated key being set to prevent repeated output of the corresponding count, the latch being then decremented on each scan. The display has a secondary character generator for characters not common to all countries.

L35 ANSWER 24 OF 39 WPIX (C) 2002 THOMSON DERWENT

AN 1982-D4618E [13] WPIX

TI Remote control for ink metering devices in rotary printing machine - disables selected devices for exclusion from commands affecting others.

DC P74 S02 S06

IN BOLZASCHUE, C A

PA (SKBA) KOENIG & BAUER AG

CYC 6

PI EP 47926 A 19820324 (198213)* DE 8p

R: FR GB IT SE
EP 47926 B2 19920513 (198213)
R: GB IT SE
DE 3034417 A 19820422 (198217)
EP 47926 B 19840912 (198437) DE
R: FR GB IT SE
US 4508034 A 19850402 (198516)
DE 3034417 C 19910117 (199103)
ADT EP 47926 A EP 1981-106927 19810904; EP 47926 B2 EP 1981-106927 19810904; US 4508034 A US 1984-575726 19840202
PRAI DE 1980-3034417 19800912
AB EP 47926 A UPAB: 19970820
The ink-metering devicedevice is controlling from a remote control unit and cooperates with a duct roller. The remote control unit has command keys for less ink and more ink for each metering device, a command key to select the required **printer** (one key for each **printer**) and command keys to select **format** and total less/more ink. The command keys are connected to a microcomputer system programmed such that after the key 'select **format**' followed by the key 'less ink' is operated for any selected **printer** than the microcomputer moves the selected ink metering device into a zero position.

Such metering devices remain in their zero positions until a manual command is given to the microcomputer and cannot be selected by any of the command keys until the manual releasing command is entered. Such zero-ed metering devices are excluded from any operation to which the remaining metering devices are subject.

L35 ANSWER 25 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1998-247185 JAPIO
TI FAULT DIAGNOSTIC SYSTEM FOR PROCESSOR
IN IIJIMA KIBOU
PA NEC CORP, JP (CO 000423)
PI JP 10247185 A 19980914 Heisei
AI JP1997-49115 (JP09049115 Heisei) 19970304
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 9
AB PURPOSE: TO BE SOLVED:To execute a self-diagnosis of a faulty processor while continuing the operation of a system by cutting off the processor from the system, in the case that a fault occures in either of the processors in a multiprocessor system.
CONSTITUTION: a fault of a processor among processors 11 to 1n is detected, system controllers 21 to 2n inhibit the processors 11 to 1n from accessing for a multiprocessor bus 30. A diagnostic mode **reset** circuit 4 displays the number of the faulty **processor** and **outputs** a **reset signal** to the system controller corresponding to the faulty processor according to a switch **input**. When the system controller transmits this **reset signal** to the processor, the faulty processor is **restarted** in a fault diagnostic mode. The faulty processor executes a self-diagnostic program stored in a ROM 5 under a local bus 20 by making a RAM 6 as a work area to output the diagnostic result to the outside through a SIO 7.

L35 ANSWER 26 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1998-039608 JAPIO
TI PICTURE IMAGE FORMING DEVICE
IN HIROBE FUMITAKE; OKI SHIGERU; IZUMIZAKI MASAMI; SAKAMI YUJI; MATSUZAKI SHIGERU; YOSHIKAWA TADANOBU; OGATA TAKAO; KITAYAMA KUNIHIKO
PA CANON INC, JP (CO 000100)

PI JP 10039608 A 19980213 Heisei
AI JP1996-192206 (JP08192206 Heisei) 19960722
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 2
AB PURPOSE: TO BE SOLVED:To obtain a high-grade color image, in which the concentration of the image is constant from the begining of the image **formation**, by detecting the concentration of a reference image in order to obtain the quantity of the supply of the toner and feeding back this result to other controllers, thereby maintaining the concentration of the toner at a constant value.
CONSTITUTION: tch image as a reference image for detecting the concentration is formed on a photo sensitive material drum 40. The light is irradiated from a light emitting part 73a of an **LED** of a concentration sensor 73, and the reflected light received by a light receiving part 73b made up of a photoelectric transfer element or the like in order to detect the actual concentration of the patch image. The output **signal** thus detected is supplied to an **input** port on one side of a comparator 75 and compared with the standard **signal**, which comes from a standard voltage **signal** source 76, which corresponds to the standard concentration of the patch image, and which is supplied to the other side of the comparator 75, in order to obtain the difference between the two and to supply the output **signal** on the difference of the concentration to the **CPU** 67. The **output signal** on the difference of the concentration is used for the control of the supply of the toner to a developer 43 within a developing machine 44, which is conducted by both a developer reflecting ATR and a video-count ATR.

L35 ANSWER 27 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1997-141974 JAPIO
TI **PRINTER** CLOCK CONTROLLER
IN SUZUKI NAOHISA
PA CANON INC, JP (CO 000100)
PI JP 09141974 A 19970603 Heisei
AI JP1995-299529 (JP07299529 Heisei) 19951117
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 6
AB PURPOSE: TO BE SOLVED:To obtain a **printer** clock controller in which the driving operation of CPU and the refresh operation of RAM are performed surely with high power saving effect through very simple circuitry.
CONSTITUTION: M access switching circuit 110 is controlled to deliver first and second refresh timing **signals** to a DRAM 60 based on the detection of first and second comparison circuits 102, 103 when first and second oscillation circuits 100, 101 are stopped and a **printer** body is turned on. A clock switching circuit 107 is also controlled to **input** a first clock to a CPU-P51 and a control function module 200 controls the **reset output** of **CPU** such that the provision of a **reset signal** is released based on the detection of the second comparison circuit 103.

L35 ANSWER 28 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1992-093790 JAPIO
TI DRIVING DEVICE OF SENSOR
IN KAI OSAMU
PA TAMURA ELECTRIC WORKS LTD, JP (CO 350937)
PI JP 04093790 A 19920326 Heisei
AI JP1990-209225 (JP02209225 Heisei) 19900809
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No.

1385, Vol. 16, No. 319, P. 113 (19920713)
AB PURPOSE: To reduce consumption of power by measuring a time required until the ON state of a light-sensing element is detected after a light-emitting element is driven, and by driving the light-emitting element thereafter in accordance with a measured value thus obtained.
CONSTITUTION: In the course of an **initializing** process executed periodically, **CPU** 1 **outputs** a **signal** of high level to an output port PO thereof at a time (t), to drive a light-emitting element 4, and receives as an **input** the ON state of a light-sensing element 5 at an **input** port PI actually through a light-sensing circuit 3, and thereby it is detected that the element 5 turns ON at the time (t) and that the **input** level thereof is put in a state of low level. While storing a time difference t2 - t1 between the drive of the element 4 and the ON state of the element 5, the CPU 1 drives the element 4 thereafter on the basis of this measured time difference t2 - t1. In other words, the time for driving the element 4 is measured actually in the **initializing** process and the element 4 is driven on the basis of this measured time for driving, so as to detect whether an object passes or not. As the result, the time for driving can be shortened and, accordingly, consumption of power can be reduced to be small.

L35 ANSWER 29 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1990-295770 JAPIO
TI IMAGE PROCESSING SYSTEM
IN SATO YUKIO; SATO YUICHI; OMURA HIROSHI; UTAGAWA TSUTOMU; SHIMIZU HIDEAKI
PA CANON INC, JP (CO 000100)
PI JP 02295770 A 19901206 Heisei
AI JP1989-117021 (JP01117021 Heisei) 19890510
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 1083, Vol. 15, No. 69, P. 103 (19910219)
AB PURPOSE: To provide high degree freedom in image processing and to simplify connection between devices by providing such mode where a **processor** provides an **output** directly to a **printer** without requiring a memory to an image processing system comprising a reader for outputting read out image data and an image data processor.
CONSTITUTION: A memory 400 comprises capacity for storing R, G, B color data and an image processing section 408 for converting the R, G, B data read out from the memory into Y, M, C, K data, where an image **signal** fed from an **input** 1 can be stored in the memory when a switcher 401 is turned to the side of a memory 403. When an output is provided directly to a **printer** without requiring a memory, YMCK **signals** can be fed to the **printer** by turning the switchers 401, 402 to through side. When a document read out section is connected through the memory 400 with an external machine 27, various **initializations** are executed upon throw-in of power source of a film reader 1 then communication with externally connected machines takes place through an interface 26 and judgement is made whether the externally connected machine is a memory or a **printer** 27.

L35 ANSWER 30 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1990-227259 JAPIO
TI LIQUID JET RECORDER
IN UTAGAWA TSUTOMU; SASAHARA KENJI; TAKAHASHI HIROYUKI; SATO YUKIO; KUMAGAI SHIGEMI; HAYASHI MASAYOSHI
PA CANON INC, JP (CO 000100)
PI JP 02227259 A 19900910 Heisei
AI JP1989-47413 (JP01047413 Heisei) 19890228

SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 1052, Vol. 14, No. 536, P. 154 (19901127)

AB PURPOSE: To reproduce a natural halftone by selecting a plurality of levels of energy to be applied to a discharge energy generator to record an **input** image **signal** based on density data of the **signal**, and performing a plurality of times of superposed recording at a recording position corresponding to the **signal** at the selected energy level.
CONSTITUTION: Parallel image **signals** of multilevels of four colors to be **input** from a digital image **signal** processor 103 to a **printer** 3 are respectively **input** in the same **format** as they are to a dither processor 301 and a quaternary circuit 302. The processor 301 converts the **input signals** into four-color binary parallel image **signals**. The circuit 302 processes the **input signals** to the quaternary parallel image **signal** for the respective colors. The four-color binary parallel **signals** processed by the processor 301 and the four-color quaternary parallel **signals** processed by the processor 302 are **input** to a dither quaternary circuit 303. The **signal** processed to '1' by the processor 103 is converted to a quaternary **signal** according to the **output** of the **processor** 302.

L35 ANSWER 32 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1988-307962 JAPIO
TI FORMING DEVICE FOR IMAGE
IN NAGATA SATOSHI
PA CANON INC, JP (CO 000100)
PI JP 63307962 A 19881215 Showa

AI JP1987-143046 (JP62143046 Showa) 19870610
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 811, Vol. 13, No. 143, P. 159 (19890407)
AB PURPOSE: To manufacture an image forming device capable of being simply set by providing a means selecting either of memory means and memorizing **initialization** data from a host position to the memory means and a setting means **initializing** the image forming device.
CONSTITUTION: When a power supply for a **printer** is turned ON, a CPU 200 sets a laser beam **printer** under an initial state. When a printing data is **input** from a host computer 210, the CPU 200 reads a character code **signal** D01, and temporarily stores the **signal** D01 in a receiving buffer 202. Numerals 205, 212 represent an initial state buffer consisting of a nonvolatile RAM, and numeral 213 represents an initial-state selecting switch selecting a currently effective initial-state buffer. When the **CPU** 200 **outputs** a character code, etc., to a code address converter 206, the address of a corresponding character pattern is output to a character generator 207, and the character generator 207 converts character data receiving at every line from a page buffer 203 into the printing **signal** of the character pattern on printing, and outputs the printing **signal** to an output interface circuit 209.

L35 ANSWER 33 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1988-059620 JAPIO
TI OUTPUT CIRCUIT
IN OKAMOTO YOSHIBUMI
PA CANON INC, JP (CO 000100)
PI JP 63059620 A 19880315 Showa
AI JP1986-202709 (JP61202709 Showa) 19860830
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 739, Vol. 12, No. 28, P. 64 (19880802)
AB PURPOSE: To execute another processing even during data output by providing a memory where output data is stored, a means where the last address of output data in this memory is stored, and a reading means which addresses the memory to read out output data.
CONSTITUTION: A clear **signal** DCL13 is outputted to **reset** a flip flop 26 and a selecting **signal** 27 is set to 0. Then, the **input** B of a selector 21 is selected and the data read out from a bit map memory 2 is outputted to a **printer** 3 through the selector 21. When a printing start instruction 11 is outputted, a printing control circuit 4 outputs an address **signal** 7 to an output circuit 2 successively with a received address as the start address synchronously with a response **signal** 8 from the **printer** 3. During this data **output**, a **CPU** in a control part 1 checks a **signal** AMAT 12 indicating the end of the output from an output circuit 2, and processings such as development of dot patterns in an image memory 5 other than direct output of printed data to the **printer** 3 is performed if the output is not terminated.

L35 ANSWER 34 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1988-059563 JAPIO
TI IMAGE FORMING DEVICE
IN NAGATA SATOSHI
PA CANON INC, JP (CO 000100)
PI JP 63059563 A 19880315 Showa
AI JP1986-202715 (JP61202715 Showa) 19860830
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 726, Vol. 12, No. 282, P. 57 (19880803)
AB PURPOSE: To form an image forming device which needs no **resetting**

even when a power supply is shut off by providing a means to set **initialization** conditions for an image forming device through a host unit and a storage means to store the **initialization** conditions to be set in nonvolatile mode.
CONSTITUTION: If a power supply switch 208 is turned ON to set a power supply in 'ON' position, CPU 200 executes an **initialization** program, setting a laser beam **printer** (LBP) to an **initialized** state. If this is terminated, **CPU** 200 **outputs** a request **signal** (RS) for any **initialization** conditions suitable for the requirements of a user to an interface circuit 201. A host computer 210 transmits **initialization** command conditions to LBP to store the conditions in an **initialization** conditions buffer 205. Further CPU 200 reads a character code **signal** D01 using an **input** interrupt processing program which is started at an interrupt **signal** S01, and stores said character code **signal** into a receiving buffer 202 temporarily. Character information which is entered in this manner is edited on a page basis by a page buffer (RAM) 203, and stored together with printing **format** control information.

L35 ANSWER 35 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1987-282322 JAPIO
TI **PRINTER** CONTROL CIRCUIT
IN NAKAJIMA YASUSHI
PA NEC CORP, JP (CO 000423)
PI JP 62282322 A 19871208 Showa
AI JP1986-126863 (JP61126863 Showa) 19860530
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 705, Vol. 12, No. 17, P. 159 (19880520)
AB PURPOSE: To relieve the load on a host device and increase the entire processing speed by outputting a data to the **printer** side through the DMA data transfer and generating part of a control **signal** by the hardware.
CONSTITUTION: A **printer** control circuit is provided with the 1st output port B6 latching an output data read from the host side memory B5, the 2nd output port applying interruption to the host **CPU**, the 3rd **output** port outputting an **initializing** **signal** **initializing** the **printer**, the 4th output port outputting a strobe **signal** to transfer a data to the **printer** by a host CPU, the 4th interruption port in the inside of a control section B4 to stop the data DMA transfer and an **input** port B7 fetching a status **signal** from the **printer**.
Further, an IO address decoder of each port and a strobe **signal** generating circuit generating a strobe **signal** to the **printer** at the DMA data transfer are included in the control section B4.

L35 ANSWER 36 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1985-262073 JAPIO
TI DISTURBANCE MONITOR FOR DIGITAL **SIGNAL** PROCESSOR
IN KAJIWARA MASANORI; TANAKA TAKESHI; NAKADE HIROSHI
PA FUJITSU LTD, JP (CO 000522)
PI JP 60262073 A 19851225 Showa
AI JP1984-118105 (JP59118105 Showa) 19840611
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 459, Vol. 1, No. 143, P. 59 (19860527)
AB PURPOSE: To enable a constant monitoring by extracting and storing **input**/output data into first and second memories to obtain the results of disturbance monitoring at the output of a means for comparing

the results with a simulation **processor** and the **output** data.
CONSTITUTION: A necessary data from an **input signal** line IL is extracted with a simulation processor 8 to be stored into a first memory 6 and a data processed with a digital **signal** processor 1 based on the data is extracted from an output **signal** line OL to be stored into a second memory 7. Then, the data of the first memory 6 is simulated with the processor 8 and the stored data controlled in the output action of the second memory 7 is compared with the results of simulation by a comparator 3. When both of the data coincide with each other, the unit 1 is **reset** while when they do not, an alarm is lighted judging that some disturbance occurs while a terminal 5 is notified thereof. This enables constant monitoring without interruption of the unit 1.

L35 ANSWER 37 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1985-056220 JAPIO
TI **OUTPUT SIGNAL PROCESSOR** FOR KARMAN'S VORTEX SENSOR
IN MITSUYASU MASAKI
PA TOYOTA MOTOR CORP, JP (CO 000320)
PI JP 60056220 A 19850401 Showa
AI JP1983-163195 (JP58163195 Showa) 19830907
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 377, Vol. 9, No. 1861, P. 91 (19850802)
AB PURPOSE: To prevent erroneous detection of flow rate by calculating flow rate in terms of average cycle and using the average cycle of the previous computation when a large cycle associated with missings of a pulse.
CONSTITUTION: A sinusoidal output **signal** of a Karman's vortex sensor 31 is fed to a waveform shaping circuit 32, where said sinusoidal **signal** is converted into a square wave **signal**. The square wave **signal** is fed to an interrupt **input** of a CPU33, which executes an interrupt routine according to the rising of the square wave **signal**. The step 402 of the interrupt routine, a value TQFX is taken in from a cunter 35, which is **reset**. Then, at the step 403, TQFX.ltoreq.K1.cntdot.TQF (K; constant) is set and when TQFX>K1.cntdot.TQF is met, missings are determined to occur in the output pulse of the waveform shaping circuit 32. Then, a shift is made directly to the step 405. At the step 405, the average cycle TQF is used to compute the air intake Q in terms of QK2/TQF. Then, the return is made.

L35 ANSWER 38 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1985-031992 JAPIO
TI PREVENTION OF ERRONEOUS ACTION IN **PRINTER**
IN KOIKE SHOJI
PA KAWAGUCHIKO SEIMITSU KK, JP (CO 365637)
PI JP 60031992 A 19850218 Showa
AI JP1983-139927 (JP58139927 Showa) 19830730
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 393, Vol. 9, No. 1581, P. 15 (19850703)
AB PURPOSE: To enable to prevent erroneous actions such as misprinting, by a method wherein an output from a driving circuit is inhibited until a power source voltage reaches a threshold voltage even when a **CPU** **outputs** a command **signal** through a misoperation.
CONSTITUTION: In the case wherein the power source voltage supplied to the CPU 1 does not reaches the threshold voltage Vth and the CPU 1 is in the condition of being **reset** by a **resetting signal** A from a reduced voltage detecting circuit 2, when the **CPU** 1 **outputs** a command **signal** X1 (X2, X3) through an

erroneous operation, an **input** (a) to an open collector 101 becomes a high-level **signal**, and the output (b) therefrom becomes OFF. In this case, since a low-level **signal** A is outputted, no electric current is passed to a transistor Tr1 through a limiting resistor R11, so that the transistor Tr1 does not operate, and a driving motor 5 in a load 4 is not driven. Accordingly, even when the CPU 1 erroneously operates in the **reset** condition to output a command **signal** X to a driving circuit 100, the load 4 is not operated, so that misprinting, erroneous paper feeding and the like are prevented from occurring.

L35 ANSWER 39 OF 39 JAPIO COPYRIGHT 2002 JPO
AN 1983-045984 JAPIO
TI HEAD DRIVE SYSTEM FOR **PRINTER**
IN AKAO AKIO
PA SANYO ELECTRIC CO LTD, JP (CO 000188)
PI JP 58045984 A 19830317 Showa
AI JP1981-146744 (JP56146744 Showa) 19810916
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 220, Vol. 7, No. 1281, P. 56 (19830603)
AB PURPOSE: To provide a drive system which can be simplified in a circuit configuration by controlling the recording start or end of a recording head specified by a specific **signal** when the comparison result of an address data with a numeric data coincide.
CONSTITUTION: A **CPU** 10 **outputs** K1 through an output port 21 to a comparator 12 upon inputting of a pulse **signal** Z, and sets the other **input** of an AND gate 23 to a high level through an output port 28. A counter 11 which is **reset** by the pulse **signal** Z counts the pulse **signals** B, and when the counted value becomes K1, the output of the comparator 12 becomes high level, the D terminal of D-FF 22 becomes high level, is then set at the timing that the pulse **signal** B becomes high level, and the Q output becomes high level. The other **input** of the AND gate 23 is high, the D-FF 29 is **reset**, and the D **input** is high.
Accordingly, when the Q output of the D-FF 22 is inverted to high, an FF 23 is set, the Q output becomes high, and the pulse **signal** Py rises.